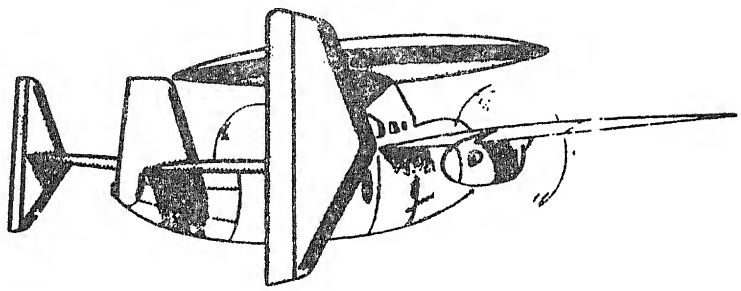
Prepared for

AVIONICS TECHNICIAN COURSE, CLASS A1

C-100-2013



UNIT 5

PROGRESS CHECK BOOKLET
VOLUME II

MODULES 4, 5, and 6

CNTT-M1109

(Rev. 7-81)

Prepared by

Naval Air Technical Training Center

Naval Air Station Memphis,

Millington, Tennessee

DECEMBER 1975

NOTE: All lesson topic progress checks (self-tests) for module 5-4 will be computer checked. You must complete a CMI answer sheet for each self-test. The student guide will list the items missed (if any) and provide your next assignment.

LESSON TOPIC PROGRESS CHECK

LIMITER CIRCUITS

Lesson Topic Learning Objectives:

1. SELECT, from a list, the statement that describes the operation of a series diode limiter.

2. SELECT, from a list, the statement that describes the operation of a parallel diode limiter.

3. SELECT, from a list, the statement that describes the operation of a saturation limiter.

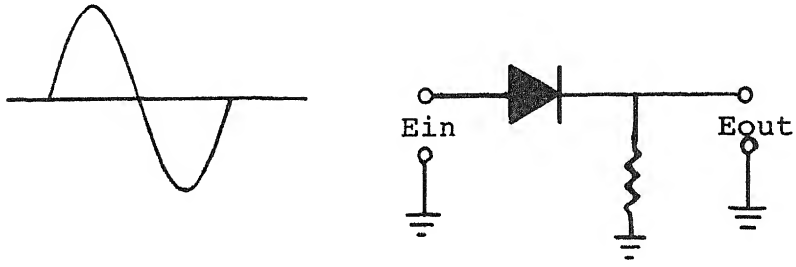
4. SELECT, from a list, the statement that describes the operation of a cutoff limiter.

5. Given a list of statements, SELECT the function of an overdriven amplifier.

6. Given a group of schematic drawings with input and output signals illustrated, SELECT the schematic of a simplified overdriven amplifier.

PROGRESS CHECK (Self-Test)

1. Select the statement that describes the operation of the series diode limiter shown below.



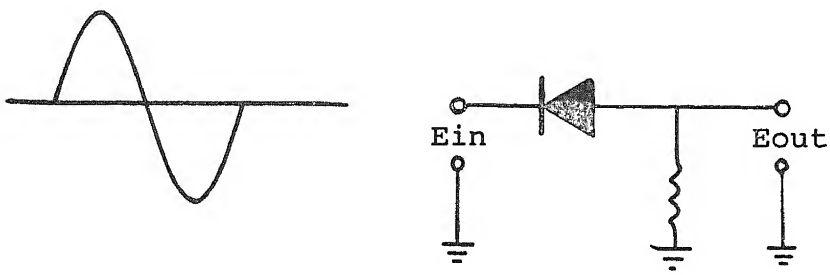
a. The negative alternation of the input signal reverse biases the diode, which limits the negative alternation of the output signal.

b. The positive alternation of the input signal reverse biases the diode, which limits the positive alternation of the output signal.

c. The negative alternation of the input signal forward biases the diode, which limits the positive alternation of the output signal.

d. The positive alternation of the input signal forward biases the diode, which limits the negative alternation of the output signal.

2. Select the statement that describes the operation of the series diode limiter shown below.



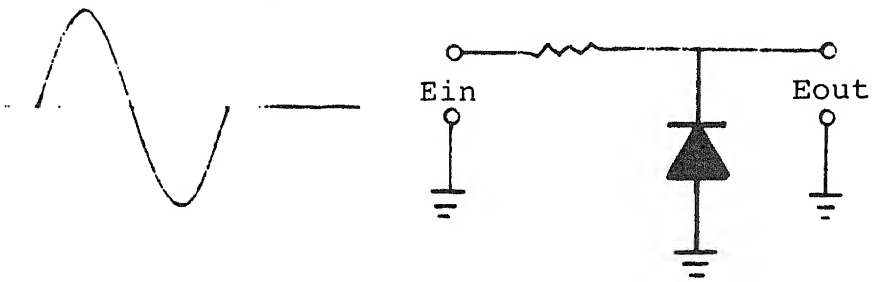
a. The negative alternation of the input signal reverse biases the diode, which limits the negative alternation of the output signal.

b. The positive alternation of the input signal reverse biases the diode, which limits the positive alternation of the output signal.

c. The negative alternation of the input signal forward biases the diode, which limits the negative alternation of the output signal.

d. The positive alternation of the input signal forward biases the diode, which limits the positive alternation of the output signal.

3. Select the statement that describes the operation of the parallel diode limiter shown below.



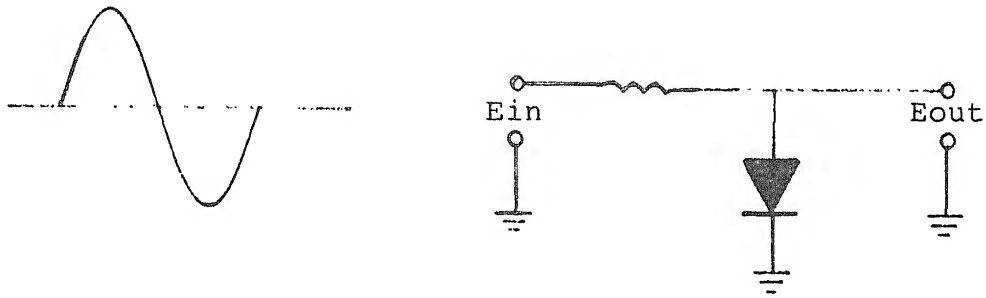
a. The negative alternation of the input signal reverse biases the diode, which limits the positive alternation of the output signal.

b. The positive alternation of the input signal reverse biases the diode, which limits the negative alternation of the output signal.

c. The negative alternation of the input signal forward biases the diode, which limits the negative alternation of the output signal.

d. The positive alternation of the input signal forward biases the diode, which limits the positive alternation of the output signal.

4. Select the statement that describes the operation of the parallel diode limiter shown below.



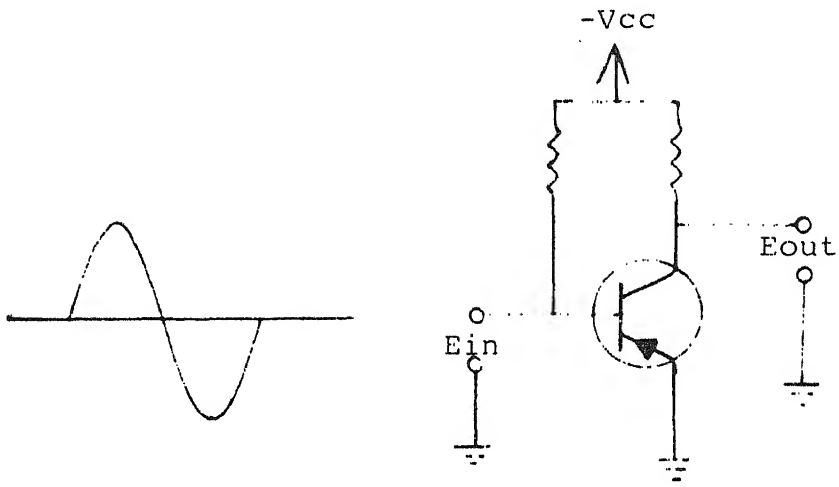
a. The negative alternation of the input signal reverse biases the diode, which limits the positive alternation of the output signal.

b. The positive alternation of the input signal reverse biases the diode, which limits the negative alternation of the output signal.

c. The negative alternation of the input signal forward biases the diode, which limits the negative alternation of the output signal.

d. The positive alternation of the input signal forward biases the diode, which limits the positive alternation of the output signal.

5. Select the statement that describes the operation of the saturation limiter shown below.



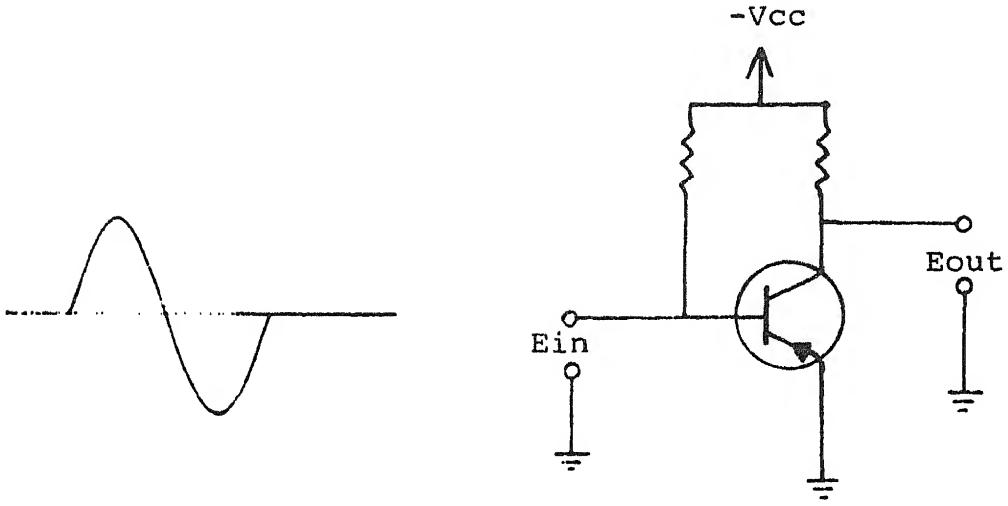
a. The negative alternation of the input signal causes the transistor to go into saturation, which limits the positive alternation of the output signal.

b. The positive alternation of the input signal causes the transistor to go into saturation, which limits the negative alternation of the output signal.

c. The negative alternation of the input signal causes the transistor to go into saturation, which limits the negative alternation of the output signal.

d. The positive alternation of the input signal causes the transistor to go into saturation, which limits the positive alternation of the output signal.

6. Select the statement that describes the operation of the cutoff limiter shown below.



a. The positive alternation of the input signal causes the transistor to go into cutoff, which limits the positive alternation of the output signal.

b. The negative alternation of the input signal causes the transistor to go into cutoff, which limits the negative alternation of the output signal.

c. The positive alternation of the input signal causes the transistor to go into cutoff, which limits the negative alternation of the output signal.

d. The negative alternation of the input signal causes the transistor to go into cutoff, which limits the positive alternation of the output signal.

7. Select the statement that describes the function of an overdriven amplifier.

   a. With a high amplitude input signal, it functions as a combination saturation and cutoff limiter.

   b. With a low amplitude input signal, it functions as a combination saturation and cutoff limiter.

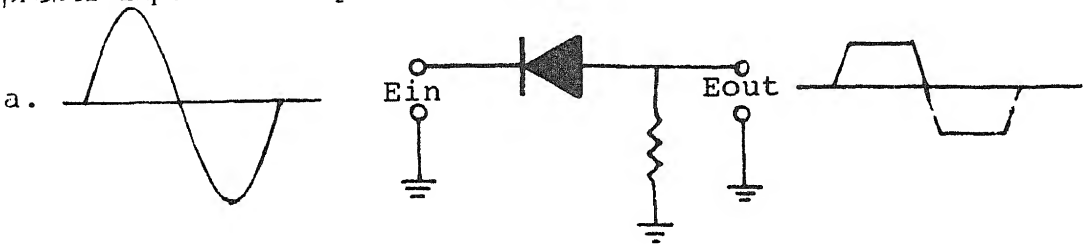
   c. With a high amplitude input signal, it functions as a Class A amplifier.

   d. With a low amplitude input signal, it functions as a mixer circuit.

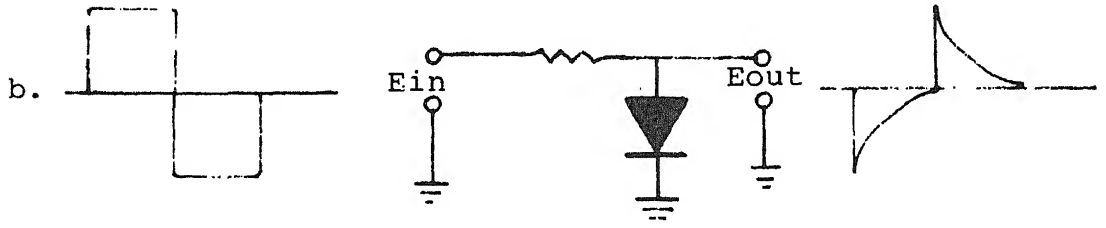
   e. Current flows for 360 degrees of the input signal, regardless of its amplitude.

8. Select the schematic of a simplified overdriven amplifier with its proper input and output waveforms.

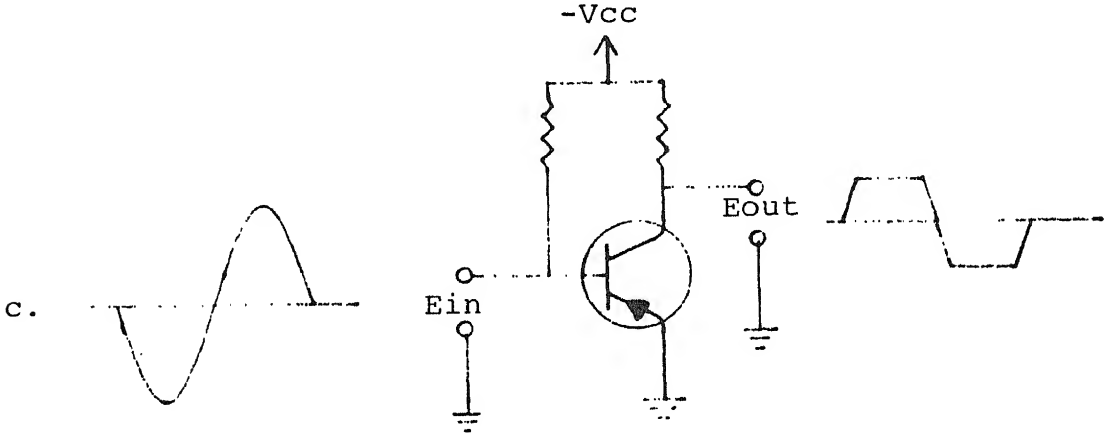
a.



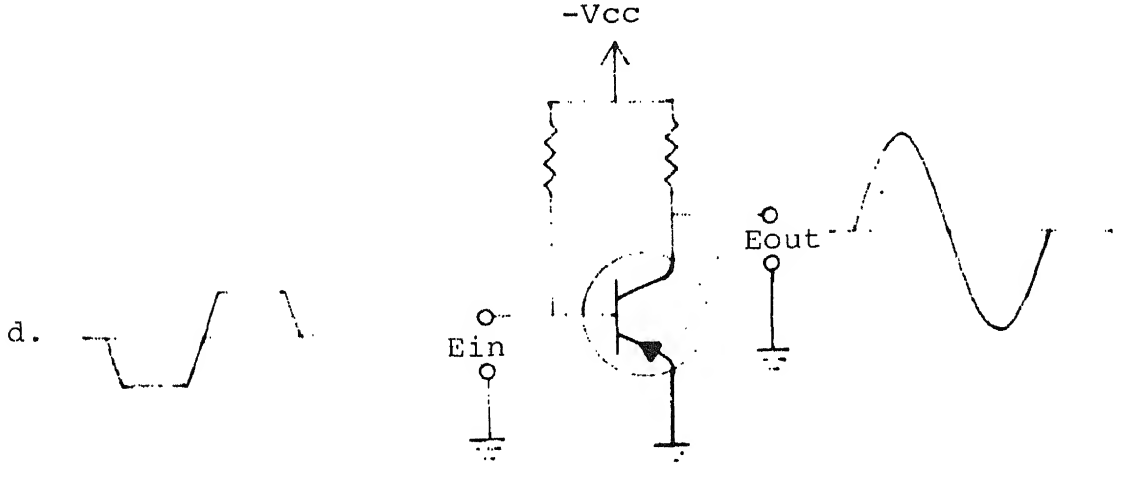
b.



c.



d.



LESSON TOPIC PROGRESS CHECK GUIDE

LIMITER CIRCUITS

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE NARRATIVE PAGE(S)	P.I. FRAME(S)
1. a	1	1
2. b	3	3
3. c	4	6
4. d	7	8
5. a	8,9	12
6. c	10	16
7. a	11	20
8. c	11,12	24

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

SIMPLIFIED MULTIVIBRATORS

1. Which of the following is the output waveform of a multivibrator?

   1. Sine waveform.

   2. Square waveform.

   3. Sawtooth waveform.

   4. Peaked waveform.

   5. Trapezoidal waveform.

2. A bistable multivibrator is a circuit which

   1. has one stable condition and one unstable condition.

   2. will remain in one of two stable conditions until triggered.

   3. has no stable states.

   4. generates square waves at twice the input frequency.

3. Select the category classification of an Eccles-Jordan multivibrator.

   1. Triggered.

   2. Free-running.

   3. Bistable.

   4. Monostable.

   5. Astable.

4. Select the type classification of a Eccles-Jordan multivibrator.

   1. Triggered.
   2. Free-running.
   3. Bistable.
   4. Monostable.
   5. Astable.

5. Select the category classification of a one-shot multivibrator.

   1. Triggered.
   2. Free-running.
   3. Bistable.
   4. Monostable.
   5. Astable.

6. Select the type classification of a one-shot multivibrator.

   1. Triggered.
   2. Free-running.
   3. Bistable.
   4. Monostable.
   5. Astable.

7. A monostable multivibrator is a circuit which:

   1. requires two inputs for a single cycle of operation.
   2. has no stable conditions.
   3. has two stable conditions.
   4. has one stable condition.
   5. requires no input trigger.

8. Select the category classification of a collector coupled multivibrator.

   1. Triggered.
   2. Free-running.
   3. Bistable.
   4. Monostable.
   5. Astable.

9. Select the type classification of a collector coupled multivibrator.

   1. Triggered.
   2. Free-running.
   3. Bistable.
   4. Monostable.
   5. Astable.

10. An astable multivibrator is a circuit which

    1. requires two inputs for a single cycle of operation
    2. has no stable conditions.
    3. has two stable conditions.
    4. has one stable conditions.
    5. requires an input trigger.

11. Select the statement which describes the primary recognition feature of an Eccles-Jordan multivibrator which distinguishes it from other types of multivibrators.

    1. The collector of each transistor is coupled to the base of the other transistor.
    2. There are two outputs available, one from either collector.
    3. The input is split and fed to both bases at the same time.
    4. The two transistors have a common emitter resistor.
    5. There is no input required to obtain a square wave out.

12. Select the condition(s) which describe the stable state(s) of an Eccles-Jordan multivibrator.

    1. Q1 conducting, Q2 conducting.
    2. Q1 conducting, Q2 cut off.
    3. Q1 cut off, Q2 conducting.
    4. Q1 cut off, Q2 cut off.
    5. Both 2 and 3 are correct.

13. Select the statement which best describes the relationship of the input frequency to the output frequency of the Eccles-Jordan multivibrator.

    1. The input frequency is twice the output frequency.

    2. The input frequency is equal to the output frequency.

    3. The input frequency has no effect on the output frequency.

    4. The input frequency is one half the output frequency.

    5. The input frequency is four times the output frequency.

14. The function of the quick coupling networks in the Eccles-Jordan multivibrator is to

    1. ensure transistor cutoff.

    2. ensure transistor conduction.

    3. provide frequency countdown.

    4. ensure rapid switching.

    5. prevent frequency countdown.

15. Select the statement which describes the recognition feature of a one-shot multivibrator which distinguishes it from other multivibrators.

    1. The collector of each transistor is coupled to the base of the other transistor.

    2. There are two outputs available, one from either collector.

    3. The two transistors have a common emitter resistor.

    4. There is no input required to obtain an output.

    5. The input is applied to both transistors at the same time.

16. Select the condition(s) which describe the stable state(s) of a one-shot multivibrator.

    1. Q1 cutoff, Q2 conducting.

    2. Q1 conducting, Q2 conducting.

    3. Q1 cutoff, Q2 cutoff.

    4. Q1 conducting, Q2 cutoff.

    5. The circuit only becomes stable when the input triggers are removed.

17. Under normal conditions the input frequency of a one-shot multivibrator

    1. is twice the output frequency.

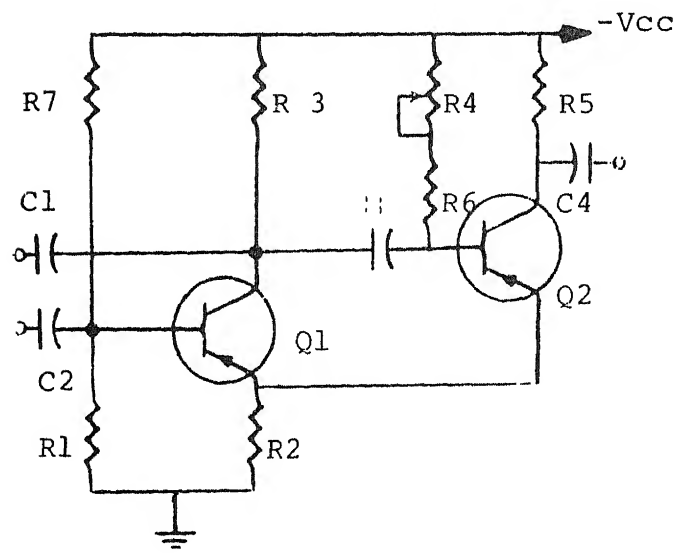
    2. has no effect on output frequency.

    3. is equal to the output frequency.

    4. is one-half the output frequency.

    5. is four times the output frequency.

18. In the circuit below, select the components which determine the output positive and negative pulse widths.



    1. R3, Q1.

    2. Q2, R6.

    3. R4, R6, C3.

    4. R3, C3, R2.

    5. R1, R7, Q1.

19. Select the statement which describes the circuit conditions required to place a one-shot multivibrator in countdown.

    1. R2 must be large enough to prevent the input from triggering Q1 into countdown.

    2. The bias voltage divider for Q1 must prevent the input from triggering Q1 into countdown.

    3. The charge time of C3 must be a long time constant.

    4. The RC time of the base circuit of Q2 must be longer than the cycle time of the input triggers.

20. Select the statement that best describes the recognition feature of a collector-coupled multivibrator (CCMV), and distinguishes it from other multivibrators.

    1. The collector of each transistor is coupled to the base of the other transistor and no input is required.

    2. There are two outputs available, one from either collector.

    3. The two transistors have a common emitter resistor.

    4. The input is applied to both transistors at the same time.

    5. The output exhibits a natural two-to-one countdown.

21. Refer to the circuit below and select the components that determine the output frequency.

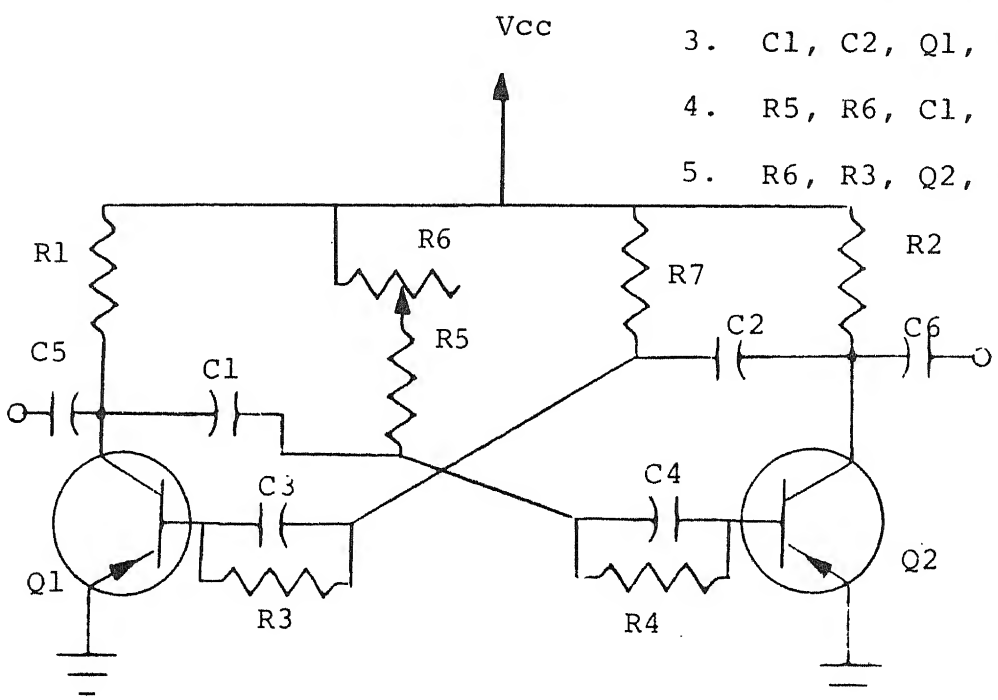
    1. C3, R3, C4, R4.

    2. Q1, Q2, R2, R4.

    3. C1, C2, Q1, R3.

    4. R5, R6, C1, R7, C2.

    5. R6, R3, Q2, C1.



    6. R1, C1, R2, C

    7. C2, C1, R2, C

22. Select the statement that best describes the purpose of returning the bases to Vcc in a collector-coupled multivibrator (CCMV).

    1. Ease of construction.

    2. To ensure rapid switching of the transistors.

    3. To improve frequency stability.

    4. To provide an increase in output amplitude.

    5. To decrease the frequency.

23. Select the statement which states the required relationship between the sync. trigger input frequency and the free-running frequency of a CCMV.

    1. The frequency of the input must be equal to the free-running frequency.

    2. The frequency of the input triggers must be lower than the free-running frequency.

    3. The input frequency must be slightly higher than the free-running.

    4. The input frequency must be twice the free-running frequency.

    5. The cycle time of the input must equal the RC time of the base circuits.

You have completed this lesson topic. Report to your Learning Supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

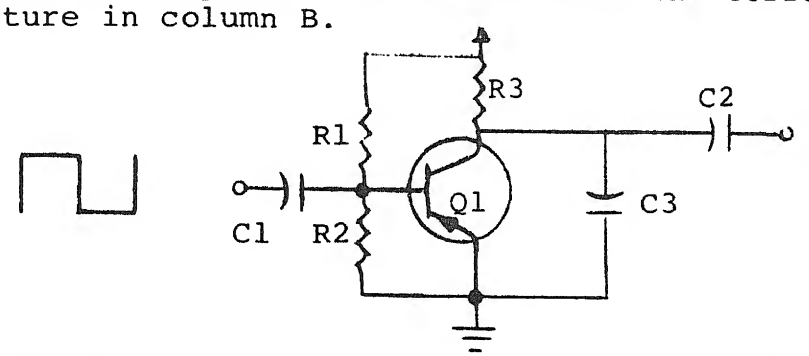
SIMPLIFIED MULTIVIBRATORS

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FRAME(s)
1. 2.			1
2. 2.			3
3. 1.			6
4. 3.			10
5. 1.			14
6. 4.			18
7. 4.			22
8. 2.			26
9. 5.			30
10. 2.			34
11. 3.			38
12. 5.			42
13. 1.			46
14. 4.			50
15. 3.			54
16. 1.			58
17. 3.			62
18. 3.			66
19. 4.			70
20. 1.			74
21. 4.			78
22. 3.			82
23. 3.			86

LESSON TOPIC PROGRESS CHECK

SIMPLIFIED SAWTOOTH AND TRAPEZOIDAL WAVEFORM GENERATORS

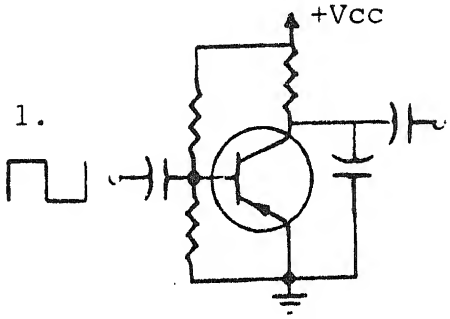
1. Match the components in column A to the correct nomenclature in column B.

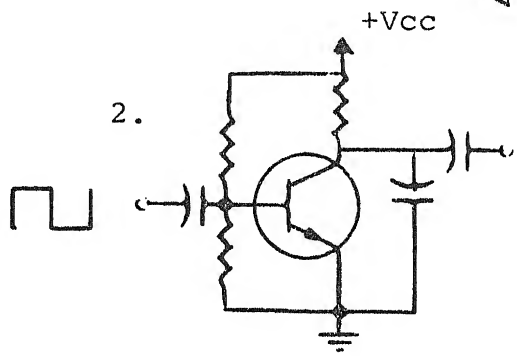


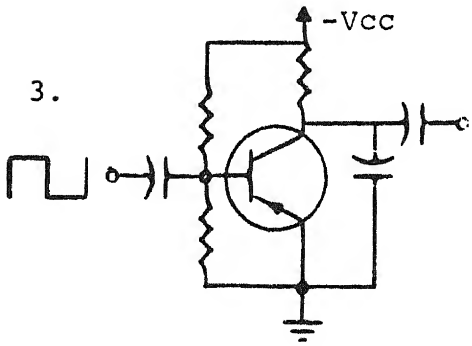
Column A	Column B
a. R1 and R2	(1) High speed switch.
b. C1	(2) Charging resistor.
c. C2	(3) Sweep capacitor.
d. R3	(4) Filter capacitor.
e. C3	(5) Input coupling capacitor.
f. Q1	(6) Base bias network.
	(7) Output coupling capacitor.
	(8) Step resistor.

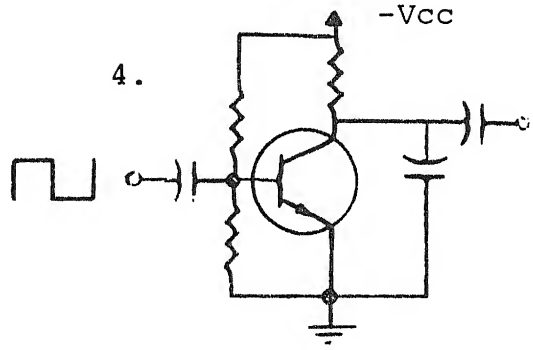
1. a6,b5,c7,d2,e3,f1.
2. a6,b7,c5,d8,e4,f2.
3. a2,b3,c4,d6,e5,f1.
4. a2,b4,c5,d8,e7,f6.

2. Select the circuit that will produce this output waveform. 

1. 

2. 

3. 

4. 

3. The output from a sawtooth waveform generator is developed across the

   1. charging resistor.

   2. sweep capacitor.

   3. charging resistor and sweep capacitor.

   4. emitter load resistor.

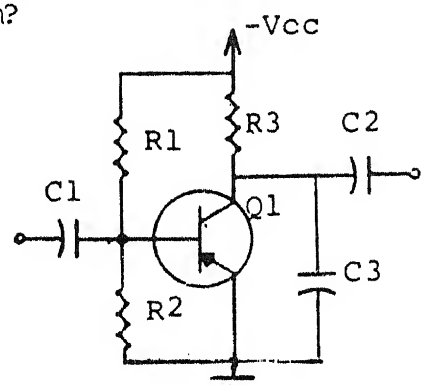
4. In the circuit below, which components determine the rate of change in the ramp of the output wavefrom?

   1. R1, C1.

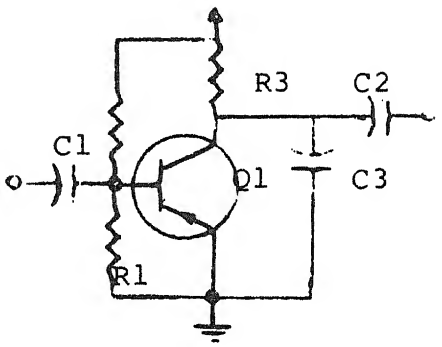
   2. R3, C2.

   3. C3, R2.

   4. C3, R3.



NOTE: Questions 5, 6, and 7 refer to the figure shown.



5. What change will occur in the output waveform if the size of C3 is increased?

   1. Fall time will decrease.
   2. Sweep time will increase.
   3. Amplitude will increase and linearity will decrease.
   4. Linearity will increase and amplitude will decrease.

6. What will be the effect on the output waveform if the size of R3 is decreased?

   1. Linearity will increase and amplitude will decrease.
   2. Fall time will decrease.
   3. Amplitude will increase and linearity will decrease.
   4. Sweep time will increase.

7. What effect will increasing the positive pulse width of the input gate to the sawtooth generator have on the output waveform?

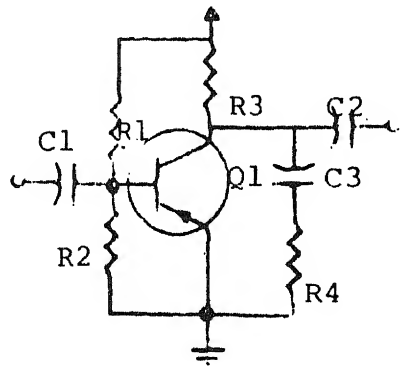
   1. Fall time will decrease.
   2. Rise time and amplitude will increase.
   3. Fall time will increase.
   4. Rise time and amplitude will decrease.

8. The step voltage of a trapezoidal waveform is developed across the

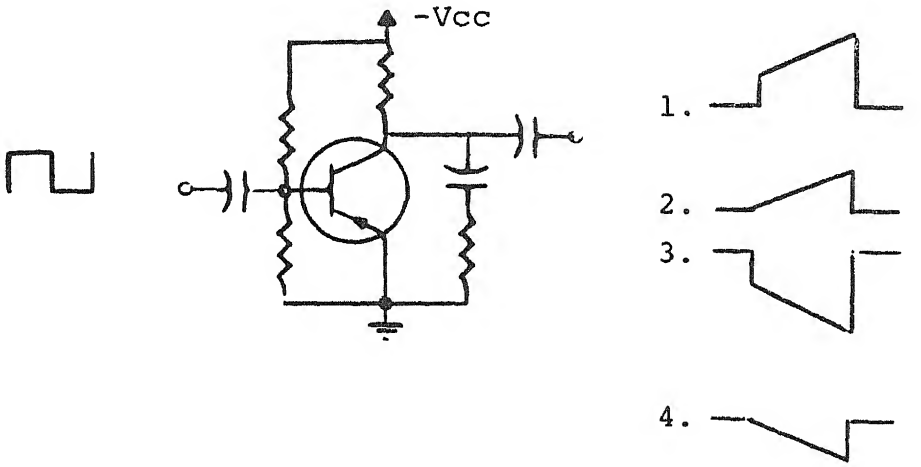
   1. step resistor.
   2. sweep capacitor and jump resistor.
   3. step resistor and charging resistor.
   4. sweep capacitor and step resistor.

9. The output waveform from a trapezoidal waveform generator is developed across the

   1. sweep capacitor.
   2. sweep capacitor and step resistor.
   3. step resistor and charging resistor.
   4. sweep capacitor, charging resistor, and step resistor.



10. Select the correct output waveform reproduced by the circuit illustrated below.



You have completed this lesson topic. Report to your Learning Supervisor for lab assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

SIMPLIFIED SAWTOOTH AND TRAPEZOIDAL WAVEFORM GENERATORS

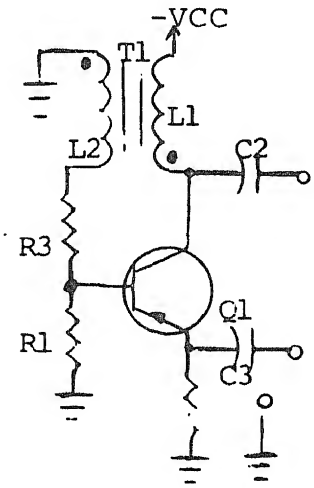
TEST ITEMS ANSWERS		PRESCRIPTIVE STUDY GUIDE		
		Summary (Page)	Narrative (Page)	P. I. (Frame)
1.	1.			1
2.	3.			3
3.	2.			6
4.	4.			10
5.	4.			17
6.	3.			19
7.	2.			22
8.	1.			29
9.	2.			31
10.	3.			34

LESSON TOPIC PROGRESS CHECK

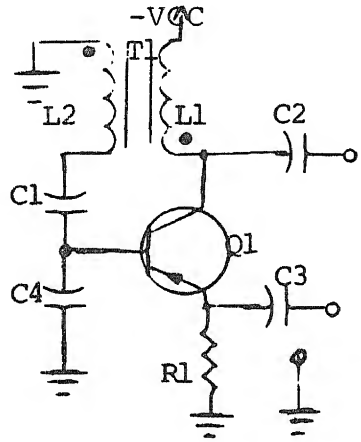
SIMPLIFIED FREE-RUNNING AND TRIGGERED BLOCKING OSCILLATOR

1. Select the schematic diagram of a free-running blocking oscillator.

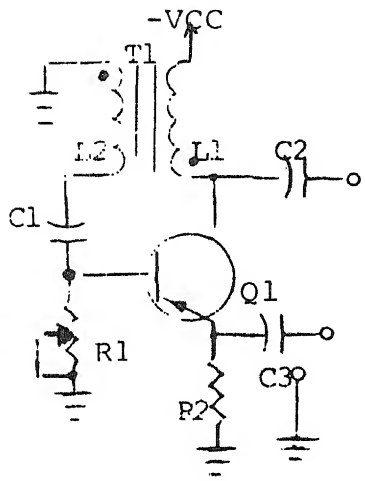
1.



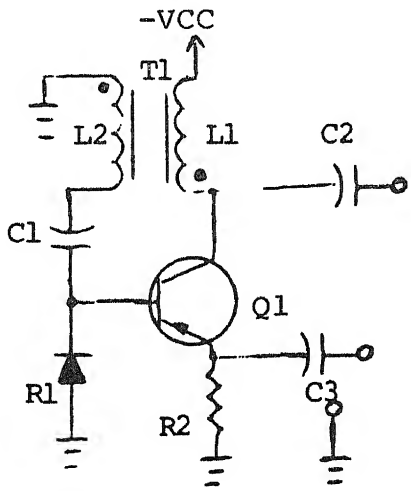
2.



3.



4.



Refer to the free-running blocking oscillator schematic diagram selected in question 1 to answer questions 2,3,4, and 5.

2. Select the statement that describes the components that primarily determine pulse width of the output.

   1. The base capacitor.

   2. The value of variable resistor R1.

   3. The values of C1 and R1.

   4. The charge path of C1 through L2, Q1 and R2.

3. What determines the transistor cutoff time in the free-running blocking oscillator.

   1. Current buildup in the primary of the pulse transformer.

   2. Current buildup in the secondary of the pulse transformer.

   3. The RC time of the base circuit.

   4. The resistance in the base circuit.

4. Which components primarily determine the output frequency of a free-running blocking oscillator?

   1. Pulse transformer.

   2. Resistor and capacitor in the collector circuit.

   3. Base coupling capacitor and T1.

   4. Base resistor R1, base capacitor C1, and L2 of the pulse transformer T1.

5. The base resistor R1 is increased in value. What is the effect on the output.

   1. PRF decreases.

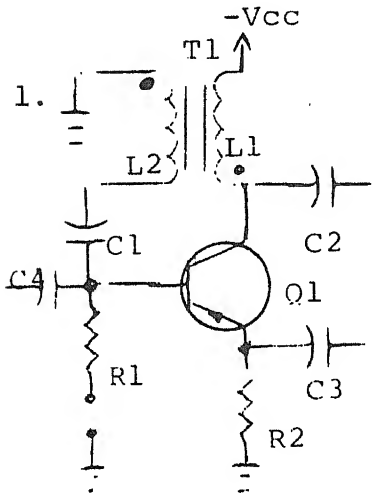
   2. PRT decreases.

   3. PRF increases.

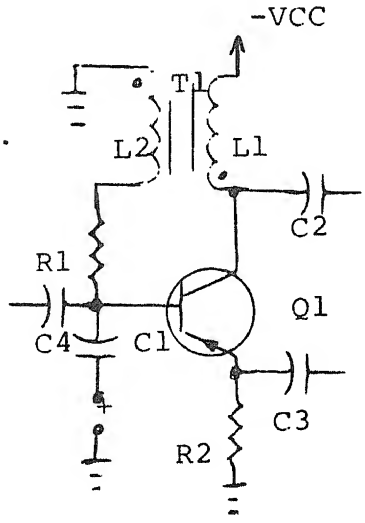
   4. Pulse width increases.

6. Select the schematic diagram of a triggered blocking oscillator.

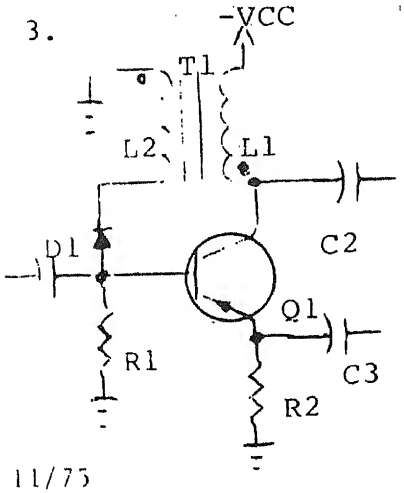
1.



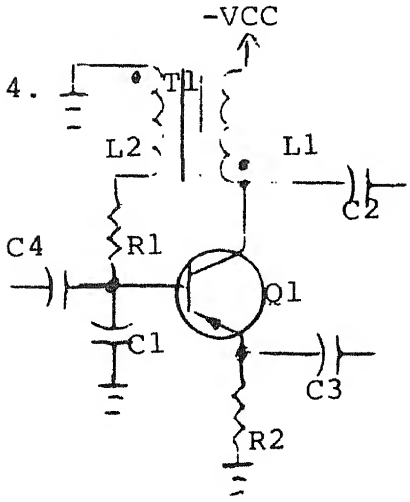
2.



3.



4.



NOTE: Refer to the triggered blocking oscillator schematic diagram selected in number 6 to answer questions 7, 8 and 9.

7. Select two statements that correctly describe the fixed bias VBB and the input trigger necessary for proper operation. (PNP transistor)

   1. The fixed bias is positive which holds Q1 cutoff.

   2. The fixed bias is negative which holds Q1 cutoff.

   3. The input trigger is positive which causes Q1 to conduct.

   4. The input trigger is negative which causes Q1 to conduct.

8. What determines the pulse width of the output from the triggered blocking oscillator?

   1. Pulse width of the input trigger.

   2. Charge time of the base capacitor C1, through L2, R2 and the base-emitter junction of Q1.

   3. Discharge of the base coupling capacitor Cc through the pulse transformer T1.

   4. Cutoff time of Q1.

9. The output frequency of a triggered blocking oscillator is determined by the

   1. amplitude of the input trigger pulses.

   2. pulse width of the input trigger pulses.

   3. RC time in the base circuit.

   4. frequency of the input trigger pulses.

You have completed this lesson topic. Report to your Learning Supervisor for lab assignment.

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ANSWERS TO PROGRESS CHECK

SIMPLIFIED FREE-RUNNING AND TRIGGERED BLOCKING OSCILLATOR

	Summary (Page)	Narrative (Page)	P.I. (Frame)
1.	3.		1
2.	4.		3
3.	3		6
4.	4		10
5.	1.		14
6.	1.		18
7.	1,4.		22
8.	2.		26
9.	4.		29

LESSON TOPIC PROGRESS CHECK
(SELF TEST)
SIMPLIFIED COUNTERS

1. Select the statement below that best describes the function of a level counter.

   1. Produces an output voltage equal to the dc average of the input.

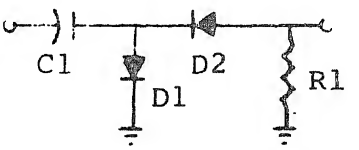
   2. Produces an output proportional to the amplitude of the input.

   3. Provides a frequency countdown.

   4. Produces an output the dc average of which is proportional to input frequency.

   5. Produces an output the amplitude of which is proportional to the input frequency.

2. Refer to the schematic below and match each component with its circuit function.



a.	C1	(1) Output developing resistor.
b.	D1	(2) Storage capacitor.
c.	D2	(3) Parallel switching diode.
d.	R1	(4) Series switching diode.
		(5) Current limiting resistor.
		(6) Charging capacitor.

1. a2,b3,c4,d1.

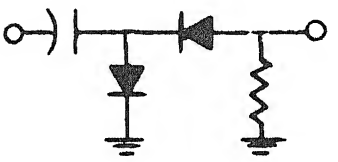
2. a2,b4,c3,d5.

3. a6,b3,c4,d1.

4. a6,b4,c3,d5.

3. Select from the following circuits the schematic of a positive level counter.

1.



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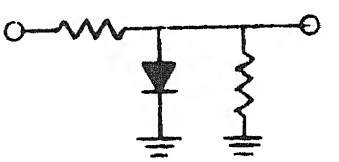
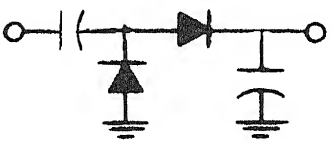


3.



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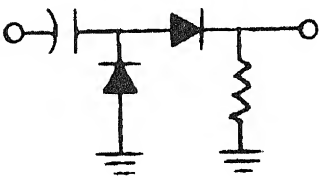
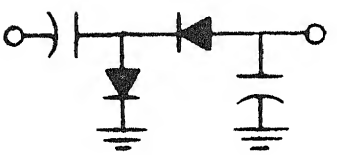
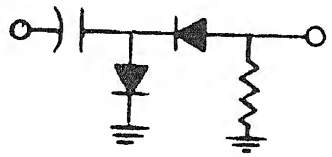


5.



4. Select from the following circuits the schematic of a negative level counter.

1.



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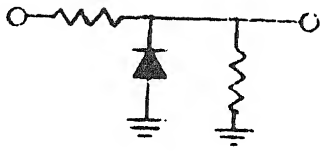
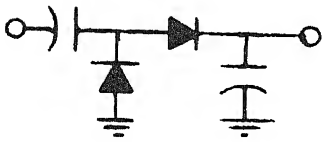
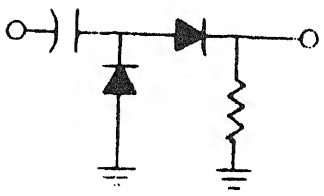


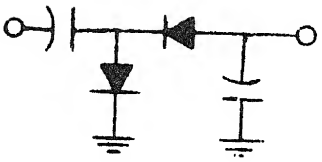
3.



4.



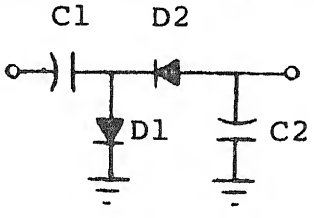
5.



5. Which of the following statements correctly describes the circuit changes which must be made to convert a level counter to a step counter.

   1. Replace the input capacitor with a resistor.
   2. Replace the output resistor with a capacitor.
   3. Change the polarity of the parallel diode.
   4. Change the polarity of the series diode.
   5. Change the polarity of both diodes.

6. Match each component listed with its circuit function.

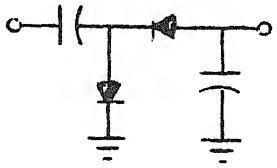


a. C1.	(1) Charging capacitor.
b. D1.	(2) Series limiting diode.
c. D2.	(3) Parallel limiting diode.
d. C2.	(4) Storage capacitor.
	(5) Parallel switching Diode.
	(6) Series switching diode.

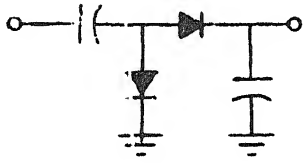
   1. a1,b5,c6,d4.
   2. a4,b3,c2,d1.
   3. a1,b3,c2,d4.
   4. a4,b6,c5,d1.

7. Select from the following circuits the schematic of a positive step counter.

1.



2.



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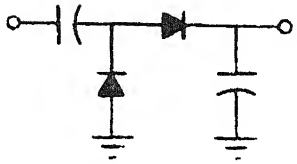
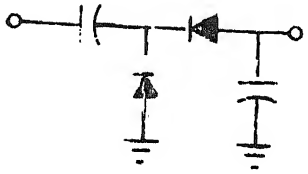
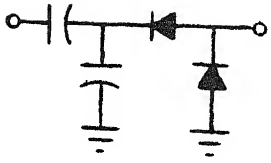


4.

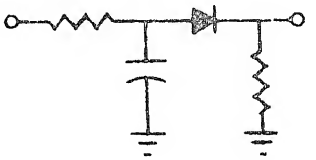


5.

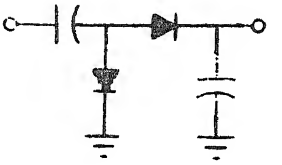


8. Select from the following circuits the schematic of a negative step counter.

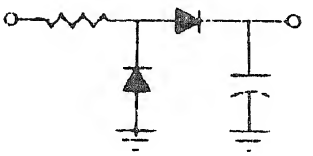
1.



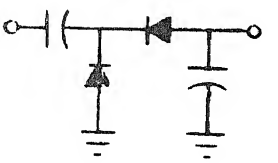
2.



3.



4.



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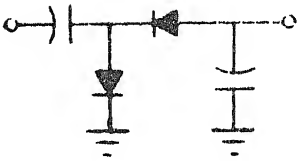


9. The purpose of connecting the output of a step counter to a triggered single-swing blocking oscillator is to provide

   1. a discharge path for the storage capacitor.

   2. frequency multiplication.

   3. an output signal from the oscillator with a dc average voltage proportional to the input frequency of the counter.

   4. frequency division.

You have completed this lesson topic. Report to your Learning Supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

SIMPLIFIED COUNTERS

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FRAME(s)
1. 4.			1
2. 3.			3
3. 4.			3
4. 1.			10
5. 2.			15
6. 1.			15
7. 3.			20
8. 5.			24
9. 4.			26

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

SIMPLIFIED CLAMPERS

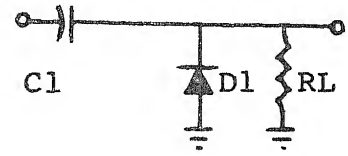
1. Match the description of clamper configurations to the correct schematic diagram.

   a. Positive clamper, positive reference.

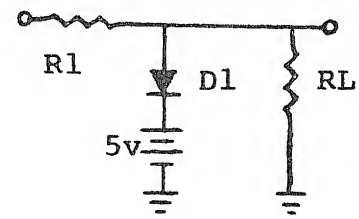
   b. Positive clamper, zero reference.

   c. Positive clamper, negative reference.

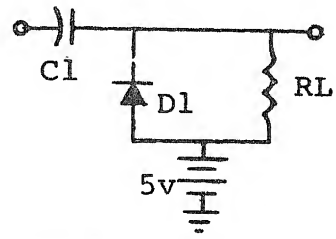
(1)



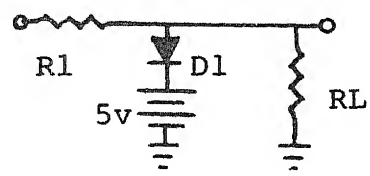
(2)



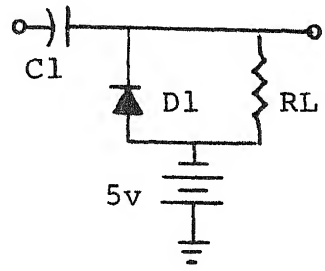
(3)



(4)



(5)



1. a3,b1,c5.
2. a5,b1,c2.
3. a2,b3,c1.
4. a5,b4,c2.
5. a3,b4,c5.

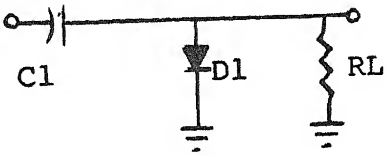
2. Match the description of clamper configuration to the correct schematic diagram.

   a. Negative clamper, negative reference.

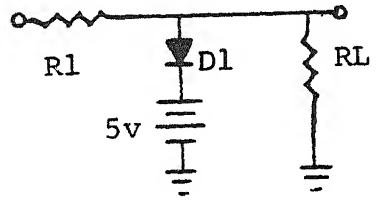
   b. Negative clamper, zero reference.

   c. Negative clamper, positive reference.

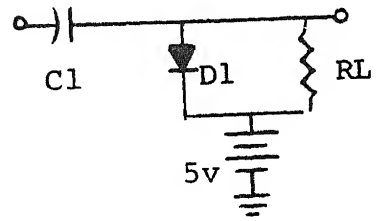
(1)



(2)



(3)



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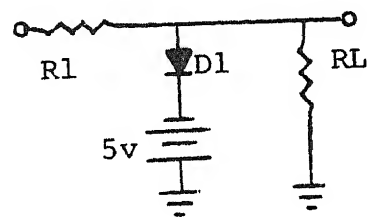

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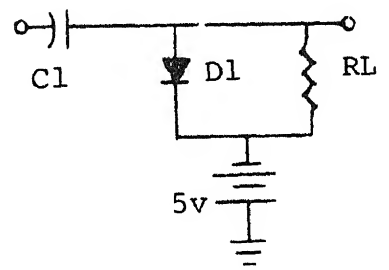


1. a1,b2,c3.
2. a3,b4,c5.
3. a5,b1,c3.
4. a3,b2,c4.
5. a5,b1,c4.

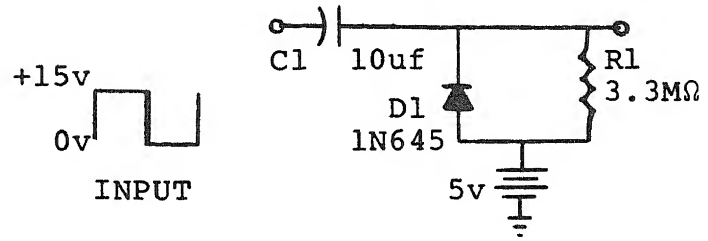
3. The function of the reference voltage in a clamper circuit is to

   1. ensure the correct level of current flow through the diode.
   2. ensure the proper direction of current flow through the diode.
   3. ensure the proper direction of current flow through the load resistor.
   4. supply power to the circuit.
   5. establish the maximum negative or maximum positive voltage reference of the output.

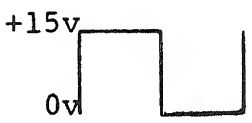
4. Select the statement that describes the charge and discharge times of the capacitor in a clamper circuit.

   1. The charge time of the capacitor is long and the discharge time is short.
   2. The charge time of the capacitor is short and the discharge time is long.
   3. Both the charge and discharge times are short.
   4. Both the charge and discharge times are long.
   5. The charge and discharge paths are equal.

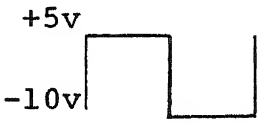
5. Select the correct output waveform of the circuit below.



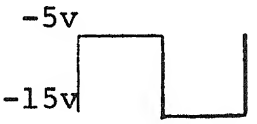
1.



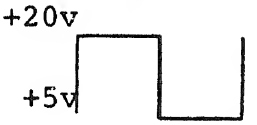
2.



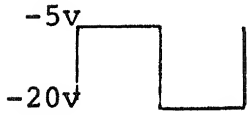
3.



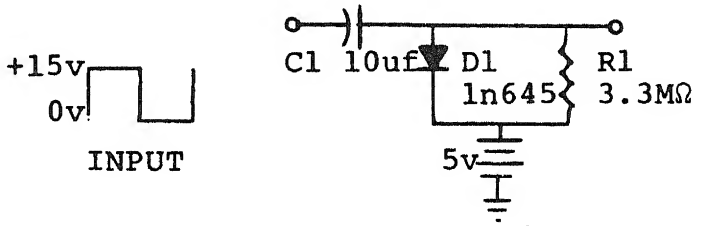
4.



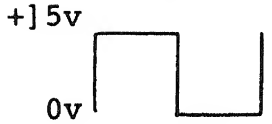
5.



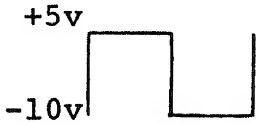
6. Select the correct output waveform of the circuit below.



1.

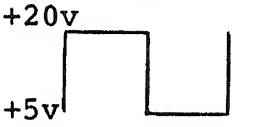


2.

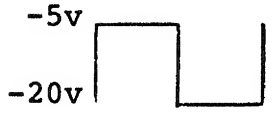


3.

4.



5.



You have completed this lesson topic. Report to your learning Supervisor for laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

SIMPLIFIED CLAMPERS

TEST ITEMS ANSWERS		PRESCRIPTIVE STUDY GUIDE		
		SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FRAME(s)
1.	1.			1 & 2
2.	3.			4 & 5
3.	5.			8
4.	2.			12
5.	4.			16
6.	2.			16

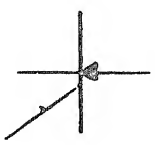
LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

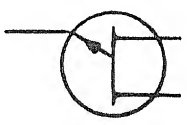
UNIJUNCTION TRIGGER OSCILLATOR

1. Select the symbol for a unijunction transistor.

a. 

b. 

c. 

d. 

2. Refer to figure 7 on the following page. Select the components that determine the shape of the output pulse from the unijunction trigger oscillator.

   a. R18, R21, and Q3.

   b. R17, R20, C11.

   c. R22, R21, and L1.

   d. R22, L1, and C11.

3. Select two statements that describe the circuit application of the unijunction trigger oscillator.

   a. Used to trigger the pulsed switching device in the modulator during transmit.

   b. Used to fire the transmitter during radar operation.

   c. Provides clock pulses to trigger the sweep gate generator during standby operation.

   d. Used to synchronize the master oscillator in the synchronizer unit.

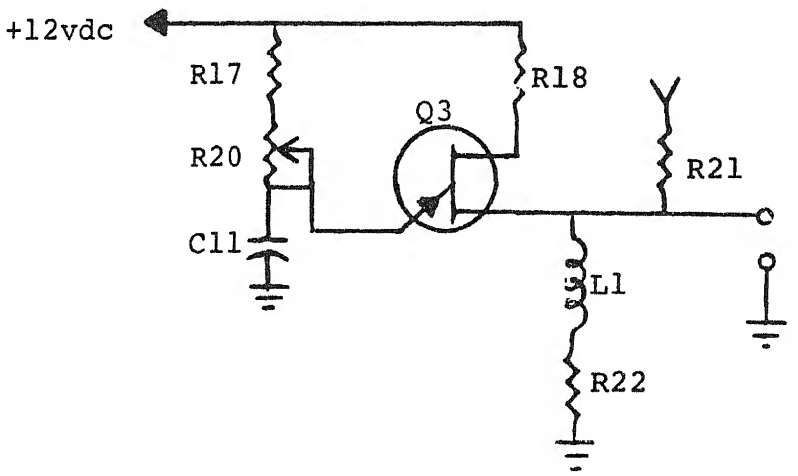


Figure 7

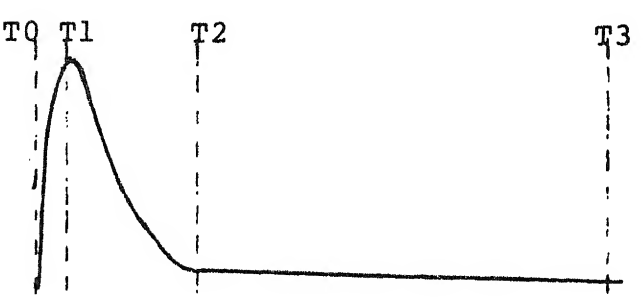


Figure 8

4. Select the statement that describes, in terms of the output waveform, the circuit function of Q3 in the unijunction trigger oscillator circuit. (Refer to figure 7 and figure 8).

   a. Q3 is a switch to provide a discharge path for C11 from T0 to T2.

   b. Q3 is a switch to complete the charge path for C11 from T0 to T2.

   c. Q3 provides flywheel path for the tank circuit from T0 to T2.

   d. Q3 amplifies the output waveform.

5. Refer to figure 7 and figure 8. Select two statements that describe the circuit functions of L1 and R22 in the unijunction trigger oscillator circuit.

   a. L1 compensates for voltage drop across R22.

   b. L1 and R22 develop the output waveform.

   c. L1 and R22 develop reverse bias for Q3 from T2 to T3.

   d. R22 provides tank circuit feedback from T0 to T2.

   e. The discharge of C11 through L1, R22, and Q3 establishes the duration of the output pulse.

6. Refer to figure 7 and 8. Select two statements that describe, in relation to output waveform, the circuit functions of C11, R20, and R17 in the unijunction trigger oscillator.

   a. C11, R20 and R17 form a variable R-C charge time network which determines the rest time of the output waveform.

   b. C11, R20 and R17 control input pulse duration.

   c. C11, R20 and R17 provide triggering voltage to drive Q3 into conduction at T0.

   d. Input pulse amplitude is controlled by C11, R20 and R17 which establishes the duration of the output pulse.

   e. C11 compensates for high voltage drops across R20 and R17.

You have completed this lesson topic. Report to your Learning Supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

UNIJUNCTION TRIGGER OSCILLATOR

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FRAME(s)
1. d.			1
2. d.			3
3. a, c.			6
4. a.			10
5. b, e.			14
6. a, c.			18

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

BOOTSTRAP SAWTOOTH GENERATOR

1. Select the signal inputs to the sweep gate generator (U1).

   a. Sync trigger.

   b. Positive sweep gate.

   c. Negative sweep gate.

   d. Sweep stop pulse.

   e. Low level sweep.

   f. Sweep control voltage.

2. Select the signal outputs of the sweep gate generator (U1).

   a. Sync trigger.

   b. Positive sweep gate.

   c. Negative sweep gate.

   d. Sweep stop pulse.

   e. Low level sweep.

   f. Sweep control voltage.

3. Q4, on the Sweep Generator Card (A3A2), functions as a/an

   a. Amplifier for the sweep gate.

   b. Isolation amplifier.

   c. Switch to turn the sweep circuit on or off.

   d. Emitter follower.

   e. Feedback amplifier.

4. Q3, on the Sweep Generator Card (A3A2), functions as a/an

   a. switch.

   b. output emitter follower.

   c. emitter follower and develops positive going sweep sawtooth.

   d. impedance matching device and current amplifier.

   e. final output amplifier for the sweep gate.

5. Q1 on the Sweep Generator Card (A3A2)

   a. functions as an emitter follower to develop the positive going sweep sawtooth.

   b. functions as a switch to turn the sweep circuit on or off.

   c. establishes the reference voltage for the sweep stop comparator (U2).

   d. establishes the timing reference for the sweep gate generator (U1).

   e. functions as an emitter follower to provide impedance matching and current gain for output low level sweep.

6. Where is the output of the bootstrap sweep generator applied?

   a. Sweep gate generator.

   b. Sweep stop comparator.

   c. Sweep resolver driver card.

   d. To a test point on the A3A2 card.

   e. X and Y Yoke Drivers.

7. The inputs to the sweep stop comparator are the

   a. negative sweep gate.

   b. positive sweep gate.

   c. dc reference voltage.

   d. low level sweep.

   e. sweep control voltage.

8. Select the statement which best describes the function of the bootstrap sweep generator.

   a. Generates a sweep gate.

   b. Determines the electrical length of the sweep.

   c. Generates a negative pulse to end the sweep.

   d. Develops a high amplitude linear sawtooth voltage.

   e. Develops a high amplitude pulse for sweep triggering.

9. Refer to the schematic diagram of the Sweep Generator Card In system operation, with 50 mile range selected, the charge path of C4 is

   a. C4, R25, R24, Range Switch and CR2.

   b. Q4, C4.

   c. Q3, C4.

   d. R9, Q3, C4.

   e. C4, R25, R24, Synchronizer Range Switch and CR2.

10. The purpose of the feedback circuit in the bootstrap sweep generator is to

    a. provide a complete charge path for C4.

    b. provide a complete discharge path for C4.

    c. provide a constant current source for the charge of C4.

    d. provide a reference voltage for the maximum sweep amplitude.

    e. shorten the charge time of C4.

11. Refer to the schematic diagram of the Sweep Generator Card. The charge path of C5 is

    a. Q3, C5, CR2.

    b. C4, Q3, C5, CR2.

    c. R9 in parallel with R1 and Q1, C5, CR2.

    d. Q4, Q3, C5, CR2.

    e. Q3, C5, R24, C4.

12. Refer to the schematic diagram of the Sweep Generator Card. Select the statement that correctly describes the relationship of the value of C5 to C4.

    a. C5 is many times smaller than C4.

    b. C5 is the same value as C4.

    c. C5 is twice the value of C4.

    d. C5 is half the value of C4.

    e. C5 is many times larger than C4.

13. During what circuit action and time period is CR2 cutoff?

    a. While C4 is discharging.

    b. While Q4 is conducting.

    c. While C5 is discharging.

    d. From T0 to T1.

    e. From T1 to T2.

14. Refer to the schematic diagram of the Sweep Generator Card. The components in the discharge path of C4 are

    a. Range Switch, R24, R25, C4.

    b. R1, and Q1 in parallel with R9, Q3, C4.

    c. CR2, C5, Q3, C4.

    d. Q4, C4.

    e. R9, Q3, C4.

15. From the start of one sweep to the start of the next sweep, the conduction levels of Q4 are:

    a. Conducting from sweep start to the end of sweep time, and cutoff from end of sweep to sweep start.

    b. Conducting throughout the cycle.

    c. Cutoff from sweep start to end of sweep time, and conducting from end of sweep to sweep start.

    d. Cutoff throughout the cycle.

    e. Cutoff from sweep start to end of sweep time, conducting from end of sweep until C4 discharges, then cutoff until sweep start.

16. During what time period does C4 charge?

    a. From sweep start to the end of sweep.

    b. From the end of sweep time to sweep start.

    c. Only when Q4 is conducting.

    d. Only when CR2 is conducting.

    e. Throughout the PRT of the radar.

You have completed this lesson topic. Report to your Learning Supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

BOOTSTRAP SAWTOOTH GENERATOR

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FRAME(s)
1. a, d.			1
2. b, c.			1
3. c.			4
4. c.			4
5. e.			4
6. b, c, d.			7
7. c, d.			11
8. d.			18
9. a.			20
10. c.			23
11. c.			27
12. e.			31
13. c, d.			34
14. d.			37
15. c.			41
16. a.			41

LESSON TOPIC PROGRESS CHECK

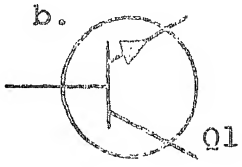
(SELF-TEST)

DIFFERENTIAL LEVEL COMPARATOR AND BIAS NETWORK

1. Refer to the sweep generator card schematic. Select the logic symbol for the integrated circuit used in the differential level comparator.

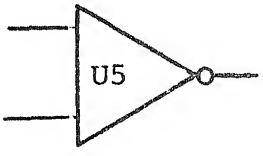
a.

b.

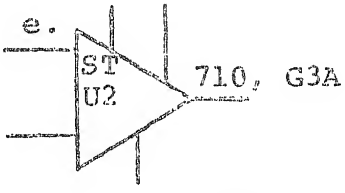


c.

d.



e.



2. Refer to the sweep generator card schematic diagram. Select the components that comprise the input circuits to the differential level comparator.

   a. C15, R1.

   b. Q1, R1.

   c. R6, R10, R14.

   d. R1, R6, R16.

   e. C1, R1, R14.

3. Select the statement that describes the function of R14 in the differential level comparator on the sweep generator card.

   a. Establishes the threshold voltage for pin 2 of comparator U2.

   b. Used to attenuate the trigger pulse at pin 2 of U2.

   c. Provides forward bias for the current stablization circuit in U2.

   d. Provides current feedback for Q1 through U2.

4. Select the statement that describes the function of U2 in the differential level comparator on the sweep generator card.

   a. Compare the sweep voltage with the threshold voltage.

   b. Compare the positive sweep gate with the negative sweep gate.

   c. Used as a digital countdown initiator.

   d. Used to establish sweep fall time.

5. Refer to the sweep generator card schematic diagram. Select the components that perform the functions of decoupling and isolation in the differential level comparator.

   a. R6, R10.

   b. C1, R11.

   c. R14, R1.

   d. R16, R6.

You have completed this lesson topic. Report to your learning supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

DIFFERENTIAL LEVEL COMPARATOR AND BIAS NETWORK

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P.I. FRAME(s)
1. e.			1
2. c.			3
3. a.			6
4. a.			10
5. b.			14

LESSON TOPIC PROGRESS CHECK

(SELF-TEST)

GATED FIELD EFFECT TRANSISTOR (FET) AND CLAMPING NETWORK

1. The three elements of the field-effect transistor are:

   a. collector.

   b. source.

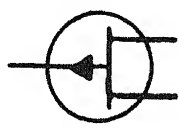
   c. gate.

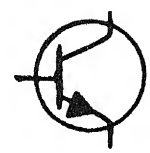
   d. base.

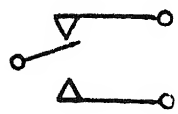
   e. drain.

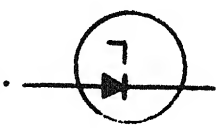
   f. emitter.

2. Which of the following is the symbol for a field-effect transistor?

a. 

b. 

c. 

d. 

e. 

3. What is the function of the field-effect transistor in the sweep clamping network?

   a. Amplifier.

   b. Electronic switch.

   c. Limiter.

   d. Gate eliminator.

   e. Servo controller.

4. What is the purpose of the field-effect transistor in the sweep clamping network?

   a. Establishes a predetermined reference for C2 at the end of sweep during NORMAL and DEPRESSED CENTER operation.

   b. Amplifies the negative sweep gate.

   c. Amplifies the sawtooth waveform applied to Q3 during DEPRESSED CENTER operation.

   d. Applies a positive voltage to C2 during NORMAL operation.

5. Select the semiconductor devices that are used in the sweep clamping network.

   a. Q2, Q3, Q9.

   b. Q8, Q9, CR5.

   c. Q9, CR3, CR5.

   d. Q8, CR3, CR5.

6. Select the electromechanical device that is used in the sweep clamping network for switching action.

   a. K1.

   b. K2.

   c. K3.

   d. CR1.

   e. TB1-6.

7. The voltage that establishes the conducting state for Q9 is the:

   a. source voltage on Q8.

   b. grid voltage on Q8.

   c. collector voltage on Q9.

   d. emitter voltage on Q2.

   e. base voltage on Q9.

8. The voltage that controls the conduction state of Q8 is the

   a. base voltage on Q9.

   b. source voltage on Q8.

   c. collector voltage on Q9.

   d. emitter voltage on Q2.

   e. base voltage on Q3.

9. Which voltage establishes the reference for C2 in the sweep clamping network?

   a. Base voltage on Q9.

   b. Source voltage on Q8.

   c. Emitter voltage on Q9.

   d. Gate voltage on Q8.

   e. Base voltage on Q2.

10. Which three of the following voltages have an effect on the sweep clamping function?

   a. Base bias on Q9.

   b. Collector voltage on Q9.

   c. Source voltage on Q8.

   d. Base bias on Q2.

   e. Emitter bias on Q2.

   f. Source voltage on Q3.

11. What are two effects of relay K3 operation on the sweep clamping functions in the Y-sweep processor card?

   a. During NORMAL sweep, K3 applies a ground potential to Q8 source.

   b. During NORMAL sweep, K3 provides a cutoff voltage for Q8.

   c. During DEPRESSED CENTER sweep, K3 provides a cutoff voltage for Q8.

   d. K3 prevents degenerative feedback to Q8 during NORMAL and DEPRESSED CENTER sweep.

   e. K3 applies a positive voltage to Q8 source during DEPRESSED CENTER sweep.

12. What are two effects that the input gating waveform has on the sweep clamping network?

    a. The negative portion of the input gate holds Q9 and Q8 cutoff.

    b. The negative portion of the input gate drives Q9 and Q8 into conduction.

    c. The positive portion of the sweep gate holds Q9 and Q8 cutoff.

    d. The positive portion of the sweep gate drives Q2 into conduction.

    e. The positive portion of the sweep gate allows Q9 to conduct which then drives Q8 into conduction.

You have completed this lesson topic. Report to your learning supervisor for lab assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

GATED FIELD EFFECT TRANSISTOR (FET) AND CLAMPING NETWORK

TEST ITEM ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P.I. FRAME(s)
1. b, c, e.			1
2. a.			3
3. b.			6
4. a.			10
5. b.			14
6. c.			18
7. e.			22
8. c.			26
9. b.			30
10. a, b, c.			34
11. a, e.			38
12. a, e.			42

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

DISPLAY-INDICATOR DEPRESSED-CENTER (OFF-SET) NETWORK

1. Select the statement that describes the purpose of the NORMAL/DEPRESSED CENTER sweep scaling network.

   a. Establishes the amplitude of the sweep voltage.

   b. Ensures that Q6 conducts from T1 to T2.

   c. Ensures that the sweep starts at the center of the CRT during depressed center operation.

   d. Establishes the sweep drive currents which determine where the sweep starts and stops on the CRT.

2. Refer to the schematic diagram of the Sweep Processor Card. Select two statements that describe the effects relay K3 has on the resolved sweep signal input to the differential amplifier.

   a. With normal selected, K3 is deenergized (pins 2, 4) and the input to Q5 is through R8.

   b. With depressed-center selected, K3 is deenergized (pins 2, 3) and the input to Q5 is through R8.

   c. With normal selected, K3 is deenergized (pins 2, 3) and the input to Q5 is through the parallel combination R8, R13, R17.

   d. With depressed-center selected, K3 is energized (pins 2, 3) and the input to Q5 is through the parallel combination R8, R13, and R17.

3. The purpose of the differential amplifier, Q5 and Q6 is to

   a. establish the quiescent current level through the constant current bias supply.

   b. provide the necessary current to the yoke drivers in normal and depressed center operation.

   c. provide the necessary current level for the Y yoke in depressed center operation only.

   d. provide the necessary current level for the X yoke driver in normal operation only.

   e. establish the necessary current level for the X and Y yoke drivers in normal operation only.

4. The function of the constant current bias supply is to maintain a constant

   a. current flow through Q5.

   b. current flow through Q6.

   c. bias voltage for Q5 and Q6.

   d. current flow through the combination of Q5 and Q6.

5. The function of the "x" and "Y" sweep feedback signals is to

   a. reduce the conduction of the sweep processor differential amplifiers.

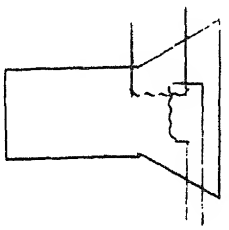
   b. provide a constant conduction level in the sweep processor differential amplifiers.

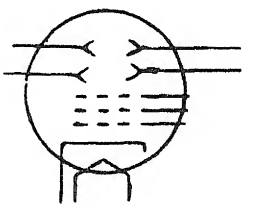
   c. provide degenerative feedback to the sweep processor differential amplifier.

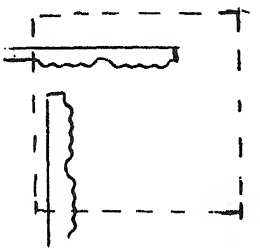
   d. keep the deflection coils from being overdriven.

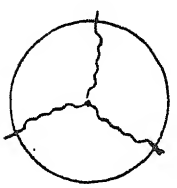
   e. provide a test point for the final sweep signal.

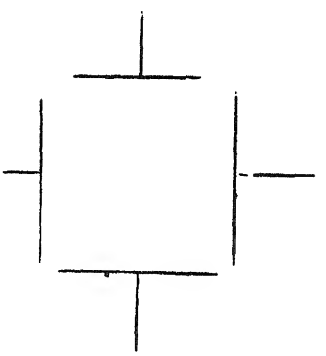
6. Select the schematic symbol below used to represent the electromagnetic deflection coils.

a. 

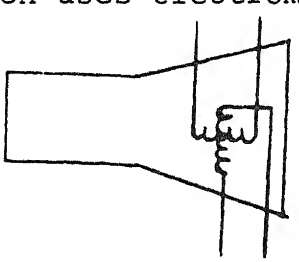
b. 

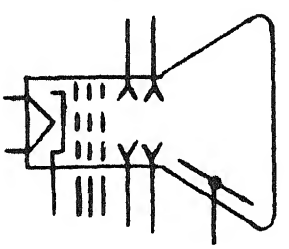
c. 

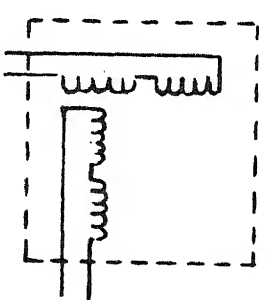
d. 

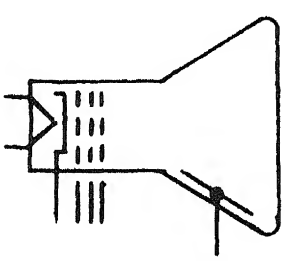
e. 

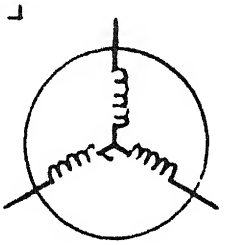
7. Which of the below is the schematic symbol for a CRT which uses electromagnetic deflection?

a. 

b. 

c. 

d. 

e. 

8. Select the signals/currents applied to the deflection coils that cause the sweep rotation in a PPI scope.

   a. A sweep voltage which varies at a sine wave rate.

   b. Two sweep currents, 90 degrees out of phase, varying at a sine wave rate.

   c. A sweep current which varies at a sine wave rate.

   d. Two sweep voltages 180 degrees out of phase varying at a sine wave rate.

   e. Two sweep currents, in phase, varying at a sine wave rate.

9. Select two directions the electron beam may be deflected when sweep currents are applied to the "X" deflection coils.

   a. To the right.

   b. To the left.

   c. Upward.

   d. Downward.

10. Select two directions the electron beam may be deflected when sweep currents are applied to the "Y" deflection coils.

   a. Upward.

   b. To the left.

   c. To the right.

   d. Downward.

You have completed this lesson topic. Report to your learning supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

DISPLAY-INDICATOR DEPRESSED-CENTER (OFF-SET) NETWORK

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P.I. FRAME(s)
1. d.			1
2. a, d.			3
3. b.			6
4. d.			10
5. c.			14
6. c.			18
7. d.			22
8. b.			26
9. a, b.			30
10. a, d.			30

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

GATED COLPITTS OSCILLATOR

1. Refer to the schematic diagram of the range marks generator card. The input network to the gated Colpitts oscillator is a:

   a. push-pull amplifier, Q3 and Q4.

   b. dual inverter, U1.

   c. three-step logic counter, U3.

   d. level comparator, U2.

2. Refer to the schematic diagram of the range marks generator card. The purpose of the input network to the gated Colpitts oscillator is to:

   a. provide gain.

   b. provide frequency division.

   c. couple the positive sweep gate to Q1 and isolate the Colpitts oscillator.

   d. triple invert the input signal without amplification.

3. Refer to the schematic diagram of the range marks generator card. Select three statements that describe the gated Colpitts oscillator.

   a. The Colpitts oscillator uses transistor Q1 with a parallel tank in the base circuit.

   b. Feedback to the dual capacitor tank is from the emitter of Q1.

   c. The output of the oscillator is taken from the emitter of Q1.

   d. The output of the oscillator is taken from pin 3 of U2.

   e. The oscillator tank uses a dual capacitor, dual inductor configuration.

4. Refer to the schematic diagram for the range mark generator. Q1 in the Colpitts oscillator circuit is used

   a. to amplify the oscillations from the tank circuit.

   b. to phase-ınvert the input square wave.

   c. to provide regenerative feedback to the tank circuit.

   d. as a saturation limiter to hold the input signal at a fixed amplitude.

5. Refer to the schematic diagram of the range marks generator card. Select the statement that describes the purpose/operation of R3 and R6 in the Colpitts oscillator.

   a. R3, R6 are used as current limiting resistors to protect Q1.

   b. R3 and R6 form a collector load resistance for Q1 and determine the dc reference of the oscillations.

   c. During the negative portion of the input pulse, R3 and R6 form a discharge path for C3 to hold Q1 cutoff.

   d. R6, R3, and C3 form a band-reject circuit to block all unwanted frequencies.

6. Refer to the schematic diagram of the range marks generator. Select the statement that describes the purpose/operation of L1, C7, C8, in the Colpitts oscillator.

   a. L1, C7, and C8 form a parallel tank to produce the 81 kHz sine wave.

   b. C7 and C8 produce opposition discharges to prevent ringing in L1 at cutoff.

   c. L1, C7, and C8 are used to compensate for bias changes due to temperature changes.

   d. L1 provides an inductive kick to double the output voltage of C7 and C8 at the collector of Q1.

You have completed this lesson topic. Report to your Supervisor for the Laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

GATED COLPITTS OSCILLATOR

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE SUMMARY PAGE(S)	NARRATIVE PAGE(S)	P.I. FRAME(S)
1. b			1
2. c.			3
3. a, b, c.			6
4. a, c.			10
5. b.			14
6. a.			18

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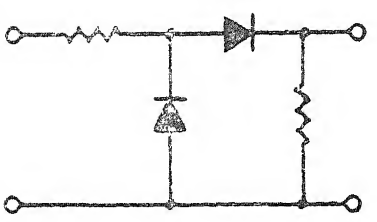
LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

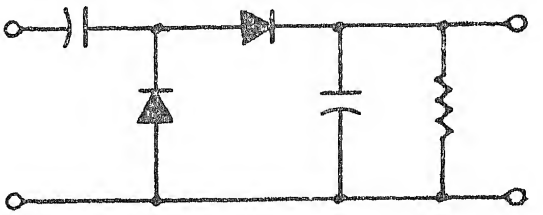
CIRCUIT ANALYSIS OF VOLTAGE DOUBLERS AND BLEEDER CIRCUITS

1. Which of the following schematics represent a half-wave voltage doubler?

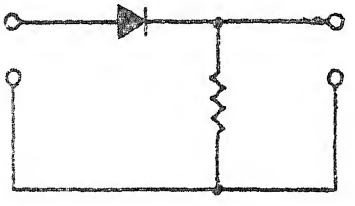
a.



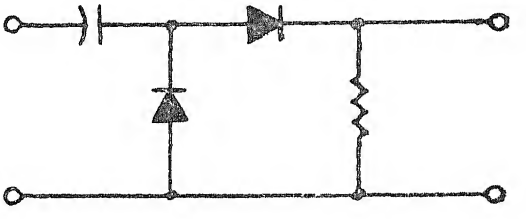
b.



c.



d.



2. Two functions of the circuit components in the half-wave voltage doubler are

   a. CR1 and CR2 provide charge paths for C1 and C2.

   b. CR1 and CR2 are used for current reduction.

   c. C1 aids the charge of C2 and the charge on C2 is the output voltage.

   d. C1 opposes C2 to prevent C2 from discharging.

3. Select three statements that describe the operation of the half-wave voltage doubler.

   a. During negative half-cycles C1 charges.

   b. C1 filters out voltage changes.

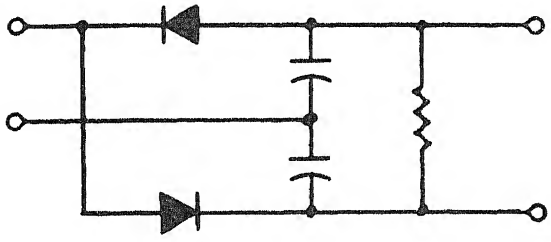
   c. During positive half-cycles C2 charges with the aid of C1 to produce a doubled voltage output.

   d. During positive half-cycles C2 charges to the potential on C1.

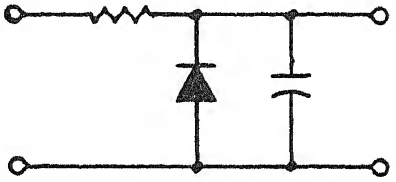
   e. During negative half-cycles C2 attempts to discharge through R1.

4. Which of the following schematics represent a full-wave doubler?

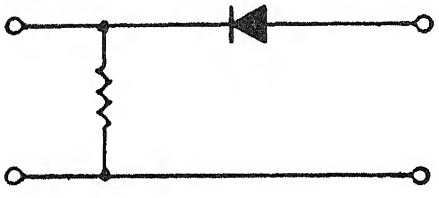
a.



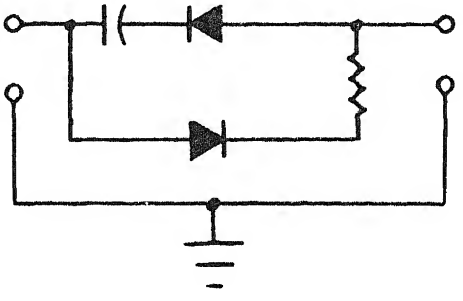
b.



c.



d.



5. The three functions/operations of the circuit components in a full-wave voltage doubler are:

   a. CR1 and CR2 provide charge paths for C1 and C2 respectively.

   b. C1 and C2 charge independently and discharge in series to produce a doubled voltage.

   c. CR1 and CR2 limit the input signal to prevent over-charging of the capacitors.

   d. C1 and R1 form a differentiator.

   e. C1 and R1 are used to provide forward bias voltage for CR2.

   f. Bleeder resistor R1 is used to provide a discharge path for the capacitors when power is removed.

6. What are three purposes of the bleeder network?

   a. Provides a discharge path for the 7 KV power supply when the radar is turned off.

   b. It provides a constant load on the 7Kv power supply.

   c. Provides voltage doubling.

   d. Voltage limiting to prevent arcing in the CRT.

   e. Provides voltage division to give 100 volts at TP-9.

   f. Provides current limiting.

7. Select two statements that describe the bleeder circuit configuration and operation.

   a. The bleeder is a parallel network of resistors.

   b. The bleeder operates as a voltage divider.

   c. A simple series of resistors forms the bleeder network.

   d. The bleeder operates as a voltage amplifier.

   d. Both parallel and series resistor combinations form the bleeder network.

You have completed this lesson topic. Proceed to the next lesson topic.

LESSON TOPIC PROGRESS CHECK GUIDE

CIRCUIT ANALYSIS OF VOLTAGE DOUBLERS AND BLEEDER CIRCUITS

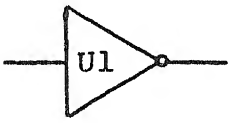
TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P.I. FRAME(s)
1. b			1
2. a, c.			3
3. a, c, e.			6
4. a.			10
5. a, b, f.			14
6. a, b, e.			18
7. b, c			22

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

DOWN COUNTERS (INTEGRATED FREQUENCY DIVIDER)

1. Refer to the schematic diagram for the Range Mark Generator Card. Select two logic symbols that represent the logic elements in the one mile range mark section of the frequency divider.

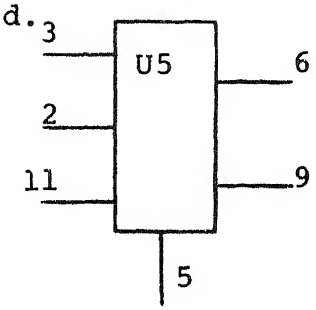
a.



b.

c.

d.



11/75

2. Refer to the schematic diagram of the Range Mark Generator Card. Logic element U7-C4A in the one-mile range mark section is

   a. a "NAND" gate used as a "NOT" function to invert the 81 kHz square wave.

   b. a "NAND" gate used to limit the amplitude of the 81 kH square wave.

   c. an inverted "OR" gate used as a "NOT" function to invert the 81 kHz square wave.

   d. an inverted "OR" gate used to limit the amplitude of the 81 kHz square wave.

3. Refer to the schematic diagram of the Range Mark Generator Card. Logic element U7-C2A in the one mile range mark section is a

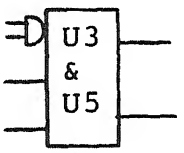
   a. "NAND" gate used to produce high outputs during high inputs.

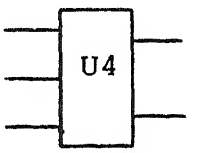
   b. "NOR" gate used to produce low outputs during high inputs.

   c. "NAND" gate used to produce low output during high inputs.

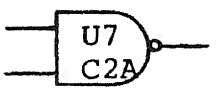
   d. "NOR" gate used to produce high outputs during high inputs.

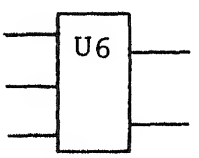
4. Refer to the schematic diagram of the Range Mark Generator Card. Select the three schematic symbols that represent the logic elements in the five mile range mark section of the frequency divider.

a. 

b. 

c. 

d. 

e. 

5. Refer to the schematic diagram of the Range Mark Generator Card. Select two statements that describe the circuit function, logic state and output of logic elements U3, U4, and U5 in the five mile range mark section. U3, U4, and U5 are

   a. inverter amplifiers.

   b. J-K flip-flops.

   c. used to invert the range marks from U2.

   d. used as a five bit counter to produce one pulse every five cycles of the 81 kHz oscillator.

6. Refer to the schematic diagram for the Range Mark Generator Card. Logic element U7-D2A in the five mile range mark section is (select two)

   a. a "NAND" gate.

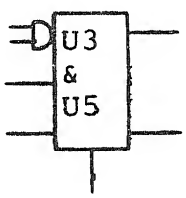
   b. an "OR" gate.

   c. used to disable the five mile range mark section to prevent the output of range marks every five miles.

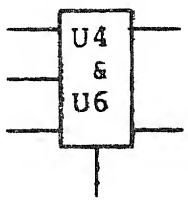
   d. used to enable the five mile range mark section and invert the output of U5.

7. Refer to the schematic diagram of the Range Mark Generator Card. Select three circuit designations that represent the logic elements in the ten mile range mark section of the frequency divider.

a.



b.



c.

d.

e.

8. Refer to the schematic diagram of the Range Mark Generator Card. Logic element U6 in the ten mile range mark section is a

   a. monostable multivibrator that produces ten range marks for every one applied to U3.

   b. J-K flip-flop that produces ten range marks for every one applied to U3.

   c. J-K flip-flop used as a 2:1 countdown device to produce one range mark for every ten range marks applied to U3.

   d. monostable multivibrator used as a 2:1 countdown device to produce one range mark for every ten range marks applied to U3.

9. Refer to the schematic diagram of the Range Mark Generator Card. Logic element U7-E2B in the ten mile range mark section is a

   a. "NAND" gate used to enable the five mile range mark section and invert the output of U6.

   b. "NOR" gate used to enable the five mile range mark section and invert the output of U6.

   c. "NAND" gate used to enable the ten mile range mark section and invert the output of U6.

   d. "NOR" gate used to enable the ten mile range mark section and invert the output of U6.

You have completed this lesson topic. Report to your Learning Supervisor for lab assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

DOWN COUNTER (INTEGRATED FREQUENCY DIVIDER)

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P.I. FRAME(s)
1. b, c.			1
2. a.			3
3. c.			6
4. a, b, c.			10
5. b, d.			14
6. a, d.			18
7. a, b, e.			22
8. c.			26
9. c.			30

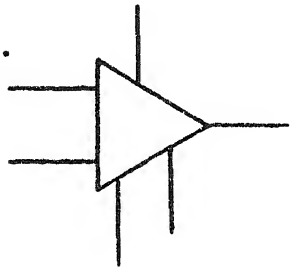
LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

MONOSTABLE MULTIVIBRATOR

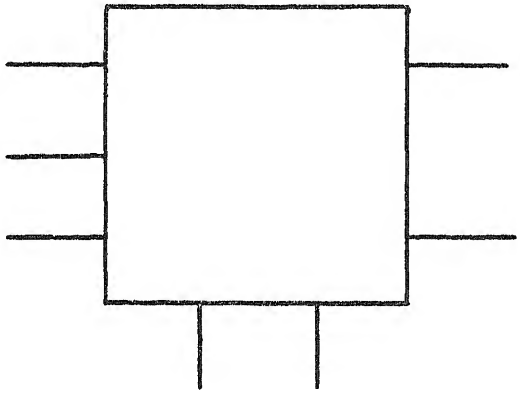
NOTE: To answer the Progress Check Questions, refer to the schematic diagram of the Range Marks Generator Card, A3A3, in the MIM.

1. Which logic symbol represents the monostable multivibrator?

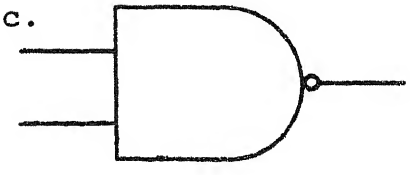
a.



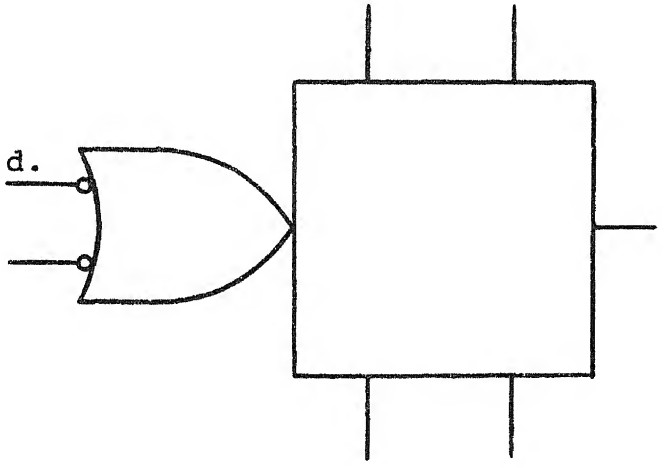
b.



c.



d.



2. Select the two external circuit components of the monostable multivibrator.

   a. U7.

   b. U8.

   c. C9.

   d. C10.

3. The function of the integrated circuit monostable multivibrator is

   a. to convert the pulses from the frequency divider network to sinewaves.

   b. to convert the pulses from the countdown circuits to useable range mark pulses.

   c. act as an inverting amplifier which changes the logic stage of the range marks.

   d. act as a pulse initiator used to extablish time references for the range marks.

4. Select the function and/or operation of the external components of the monostable multivibrator. (Select two)

   a. C10 is used to provide wave-shaping and determines the output pulse width.

   b. C9 is used to filter out ac ripple from the input pulses.

   c. C10 is used to block dc voltages from pin 11 of U8.

   d. C9 is used to filter out any possible ripple on the positive 5 volt supply voltage.

   e. C10 is used as an integrating capacitor to waveshape the input pulses.

5. The voltage needed to trigger the monostable multivibrator is a

   a. constant high voltage.

   b. high-to-low changing voltage.

   c. constant low voltage.

   d. low-to-high changing voltage.

6. Select the statement that describes the voltage-to-logic relationship in the monostable multivibrator.

   a. Negative voltage is a low and zero voltage is a high.

   b. Negative voltage is a high and zero voltage is a low.

   c. Positive voltage is a high and zero voltage is a low.

   d. Negative voltage is a low and positive voltage is a high

7. Select the statement that describes how a high-to-low change in the input affects the output of the monostable multivibrator.

   a. The output is a positive pulse one microsecond in duration.

   b. During the input change, the output is a sinewave oscillation.

   c. A change of high-to-low and a return to high occurs on the output during high-to-low changes at the input.

   d. A high-to-low change at the input causes the output to go from low-to-high and remain there until the high-to-low change at the input.

You have completed this lesson topic. Report to your Learning Supervisor for lab assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

MONOSTABLE MULTIVIBRATORS

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FRAME(s)
1. d.			1
2. c, d.			3
3. b.			6
4. a, d.			10
5. b.			14
6. c.			18
7. a.			22

LESSON TOPIC PROGRESS CHECK

PROPER HANDLING AND DISPOSAL OF CATHODE RAY TUBES

1. Select the three safety precautions an individual should observe when disposing of a cathode-ray tube.

   a. Prevent the chemical coating on the inside face of the CRT from coming in contact with the hands or the skin.

   b. Stand on a rubber mat while handling the tube.

   c. Stand in front of the tube to minimize the danger of implosion.

   d. Never stand directly in front of the tube.

   e. Wear protective glasses and gloves.

   f. Wear ear plugs to minimize noise in the event of implosion.

2. Select four safety precautions that are related to the care of cathode-ray tubes?

   a. Use only moderate pressure when securing the clamps to hold the tube in place.

   b. Hold or carry the tube only by its neck.

   c. Avoid any contact of the tube with sharp or hard objects.

   d. Break the vacuum seal prior to installation of the cathode-ray tube.

   e. Hold or carry the tube with both hands.

   f. Never carry or hold the tube by its neck.

   g. Coat the face of the tube with the proper chemical to prevent implosion.

3. Select the statement that describes the proper method to use when removing a CRT.

   a. Hold the CRT with only one hand on the neck of the tube and gently slide the CRT from the socket.

   b. Hold the CRT with both hands on the face of the tube and gently slide the CRT from the socket.

   c. Clamp a holder to the neck of the CRT and remove the tube quickly.

   d. Hold the CRT with both hands on the neck of the tube and gently slide the CRT from the socket.

4. Select three statements, in the proper order, that correctly describe the procedure for removing the danger of implosion from a CRT before disposal.

   a. Place the defective CRT face up, in an empty container.

   b. Place the defective CRT, face down, in an empty CRT carton.

   c. Carefully break off the locating pin on the tube base.

   d. Break the vacuum seal of the CRT with a screwdriver or a pair of pliers.

You have completed this lesson topic. Proceed to the next lesson topic.

LESSON TOPIC PROGRESS CHECK GUIDE

PROPER HANDLING AND DISPOSAL OF CATHODE-RAY TUBES

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FRAME(s)
1. a, d, e.			1
2. a, c, e, f.			3
3. b.			6
4. b, c, d.			10

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

THREE PHASE POWER SUPPLY AND OVERLOAD PROTECTION CIRCUITRY

1. Select the statement that describes the purpose of an ac indicating fuseholder.

   a. Provides a 30 second delay before a fuse opens.

   b. Provides a visual indication of a good or bad fuse in an ac circuit.

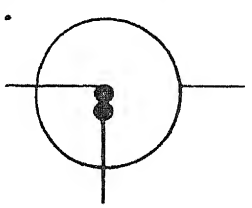
   c. Provides a visual indication of a good or bad fuse in a dc circuit.

   d. Senses the high voltage overload.

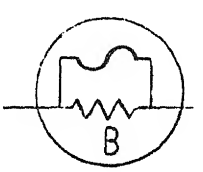
   e. Compensates for surges of input current.

2. Select the schematic symbol for an ac indicating fuseholder.

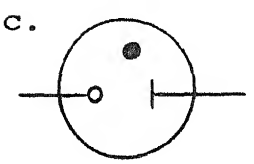
a.



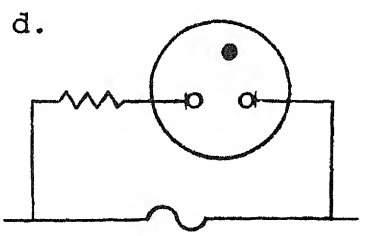
b.



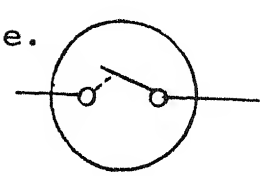
c.



d.



e.



3. Select the statement that describes the purpose of the thermal time delay relay.

   The thermal time delay relay provides a

   a. 45 second delay of output voltage to the high voltage circuitry.

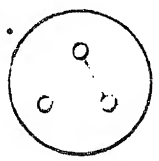
   b. 30 second delay of input voltage to the high voltage circuitry in the display-indicator and the modulator.

   c. means of monitoring the high voltage output.

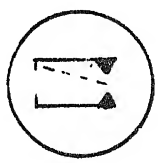
   d. bleeder path for the high voltage power supply.

4. Select the schematic symbol for a thermal time delay relay.

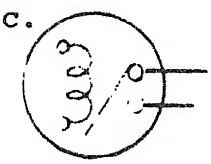
a.



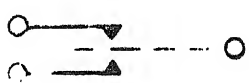
b.



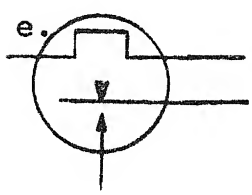
c.



d.



e.



5. Select the statement that describes the purpose of a dc indicating fuseholder.

   a. Senses the inverse current in the overload circuit.

   b. Provides a bleeder path for the low voltage power supply.

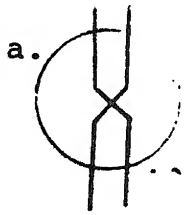
   c. Provides a visual indication when the fuse is good or bad.

   d. Provides a 30 second time delay for the high voltage circuit.

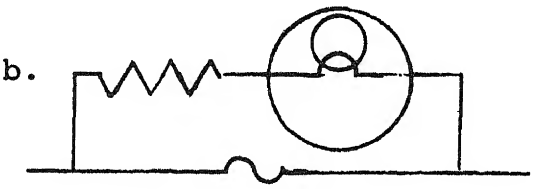
   e. Provides a visual indication of a good or bad fuse in an ac circuit.

6. Select the schematic symbol for a dc indicating fuseholder.

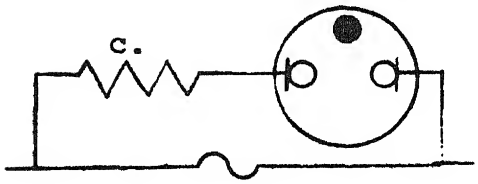
a.



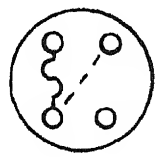
b.



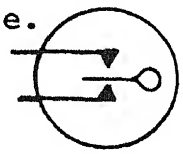
c.



d.



e.



7. The purpose of the three-phase, full-wave rectifier is to

   a. cause the overload relay K1 to energize.

   b. provide an attenuated measurement point for the 300Vdc.

   c. filter out voltage variations in the emitter of Q1.

   d. produce a +dc output voltage from the 208Vac three-phase input.

8. Refer to the schematic diagram of the high voltage power supply. Which of the following components are in the three-phase, full-wave rectifier circuit?

   a. VR6, VR7, Q3, A4.

   b. CR5 through CR8.

   c. CR1 through CR4.

   d. CR4 through CR9.

9. The purpose of the overload protection circuit is to

   a. remove the 100Vac from the modulator when the applied voltage exceeds the predetermined value.

   b. supply a ground to energize the HV ON and STDBY indicator lights.

   c. remove the 300vdc from the modulator when the applied voltage exceeds the predetermined value or when an overload exists in the PFN.

   d. energize the thermal time delay circuit.

   e. provide protection for the power supply when a mismatch occurs within the PFN, magnetron, or waveguide sections.

10. Refer to the schematic diagram of the modulator power supply, figure 2-21.

    The components included in the overload protection circuitry are

    a. Q1, R5, K1, R2.

    b. CR1 through CR4.

    c. Q2, VR3, R10, R11, R3.

    d. CR4, CR8, C1, T4, R2.

11. Refer to the schematic diagram of the modulator power supply.

    Select the components in the inverse current sensing circuit.

    a. Q1, CR4, L1, R5.

    b. K4, R4, CR1, CR2.

    c. A6A1A4CR2, meter M2, A6A1K3.

    d. A6A1M4, T7, A6A1A1Q2

12. When the radar is operating properly, the reading on the inverse current meter will be

    a. 0.4ma or more.

    b. 0.2ma or less.

    c. 0.4ma or less.

    d. 0.2ma or more.

    e. 3.0ma or more.

13. Refer to the schematic diagram of the modulator power supply.

With more than 0.2ma of inverse current in the inverse current network (select two).

a. A6A1A2K2 energizes.

b. High voltage relay K1 (A6A1A2K1) energizes.

c. K8 energizes.

d. Relay K3 (A6A1A2K3) energizes.

e. Relay K2 (A6A1A2K2) de-energizes.

14. Refer to the schematic diagram of the modulator power supply.

When A6A1A2K1 de-energizes, the high voltage is removed from the charging circuit of the

a. 1kHz oscillator.

b. pulse transformer.

c. pulse forming network.

d. STC circuit.

e. dual TR tube.

You have completed this lesson topic. Report to your Learning Supervisor for lab assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

THREE PHASE POWER SUPPLY AND OVERLOAD PROTECTION CIRCUITRY

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P.I. FRAME(s)
1. b			1
2. d.			3
3. b.			5
4. e.			8
5. c.			11
6. b.			14
7. d.			17
8. d.			20
9. c.			23
10. a.			26
11. c.			29
12. b.			32
13. a, d.			35
14. c.			38

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

PULSE FORMING NETWORK AND SCR CONTROL CIRCUITS

1. The purpose of the pulse forming network as used in the pulse type radar is to

   a. generate trigger pulses for the time delay.

   b. supply the basic 1kHz timing pulse.

   c. develop a high voltage dc pulse to be applied to the pulse transformer.

   d. develop a high voltage ac pulse to be applied to the pulse transformer.

2. Two properties of transmission lines that are combined to form an artificial line are

   a. series inductance, series capacitance.

   b. parallel inductance, series capacitance.

   c. series inductance, shunt resistance.

   d. shunt capacitance, parallel inductance.

   e. series inductance, shunt capacitance.

3. Which components in the PFN affect the shape and duration of the output pulse? (Select two.)

   a. Resistors.

   b. Capacitors.

   c. Inductors.

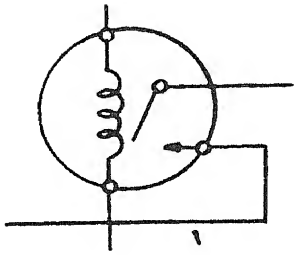
   d. Transistors.

   e. Relays.

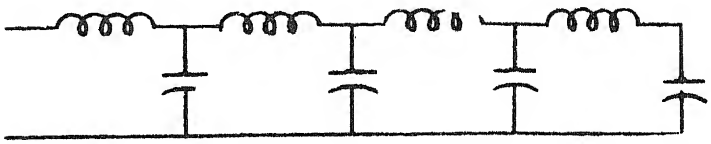
   f. Diodes.

4. Select the symbol of a Pulse Forming Network.

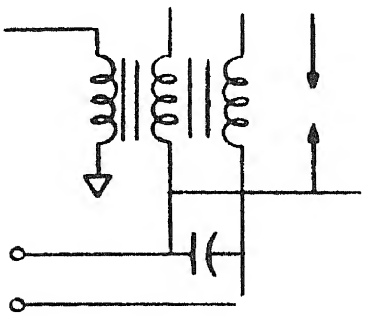
a.



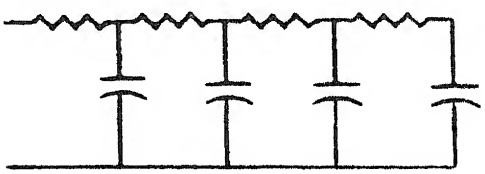
b.



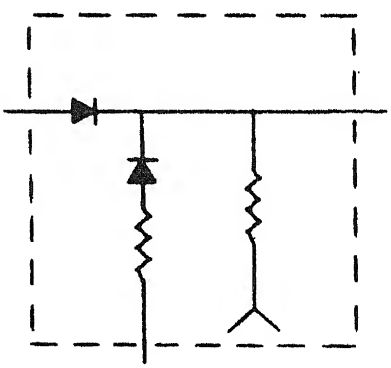
c.



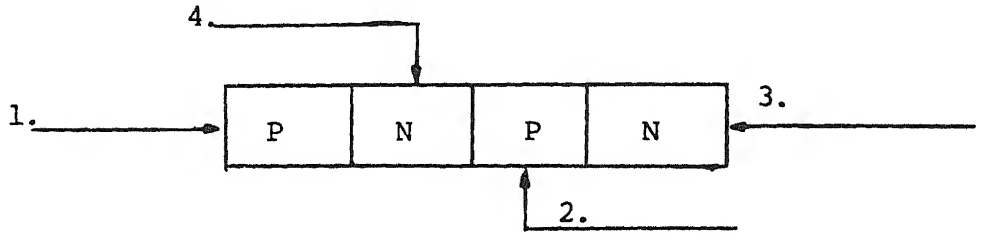
d.



e.



5. Select the location of the anode, gate and cathode of an SCR.



a. 1-cathode, 2-gate, 3-anode.

b. 1-cathode, 2-gate, 4-anode.

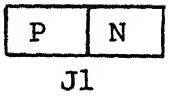
c. 1-anode, 2-cathode, 3-gate.

d. 1-anode, 2-gate, 3-cathode.

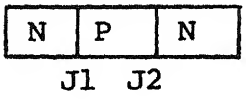
e. 1-gate, 2-anode, 4-cathode.

6. Select the correct block illustration that represents the structure of an SCR.

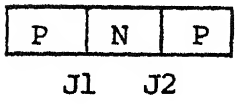
a.



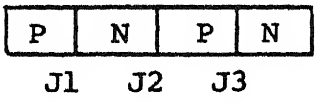
b.



c.



d.



7. Refer to figure A and select the method(s) of bias that is/are required to properly bias an SCR for cutoff.

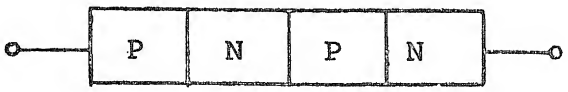
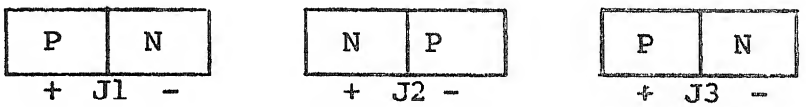
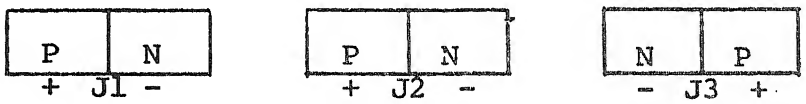


FIGURE A

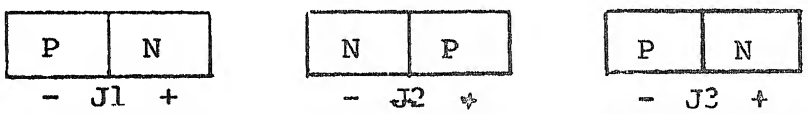
a.



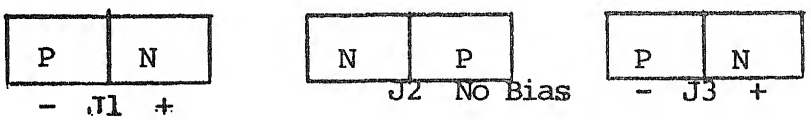
b.



c.

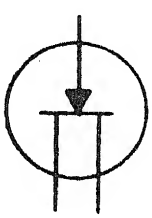


d.

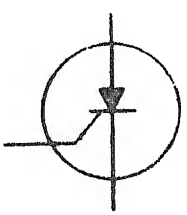


8. Select the schematic symbol for an SCR from the list below.

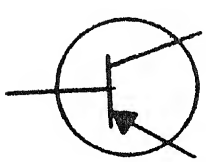
a.



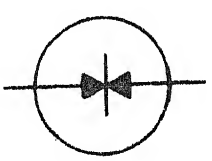
b.



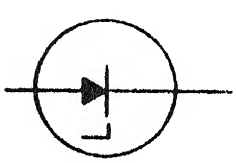
c



d.



e.



9. Select three statements that describe the electrical properties of an SCR.

   a. It has unidirectional current flow.

   b. The anode must be positive with respect to the cathode.

   c. The anode must be negative with respect to the cathode.

   d. Conduction and cutoff can be controlled by proper biasing.

   e. A negative pulse applied to the gate will cause conduction.

10. Select two statements that describe why SCRs are utilized in radar modulators.

   a. The SCR can be used as an electronic switch.

   b. The SCR can be used to provide a discharge path for the pulse forming network (PFN).

   c. The SCR allows the pulse transformer to charge continuously.

   d. The SCR permits operation of the overload relays.

11. Select the reference designators for the SCR and for the Control Circuitry card.

   a. A6A1Q1, A6A1A2

   b. A6A1Q1, A6A2A1

   c. A6A1Q1, A6A1A3

   d. A6A1Q1, A6A1A1

   e. A6A1Q1, A6A1A4

12. Select the statement that describes the function of the SCR control circuitry.

    a. +28 vdc initiates operation of Q1 in the SYS OPN mode.

    b. In the SYS OPN mode, the 1 kHz clock trigger is applied directly to the SCR.

    c. It requires no additional circuitry to function.

    d. It limits the voltage applied to the spark gap.

13. The SCR conducts to discharge the PFN when

    a. provided with 28 vdc pulse from the synchronizer.

    b. K3 becomes energized.

    c. the Hv terminates.

    d. a 1 kHz clock trigger is applied to the gate.

14. Select two statements that describe the function of the charging inductor L1.

    a. Permits operation of K3.

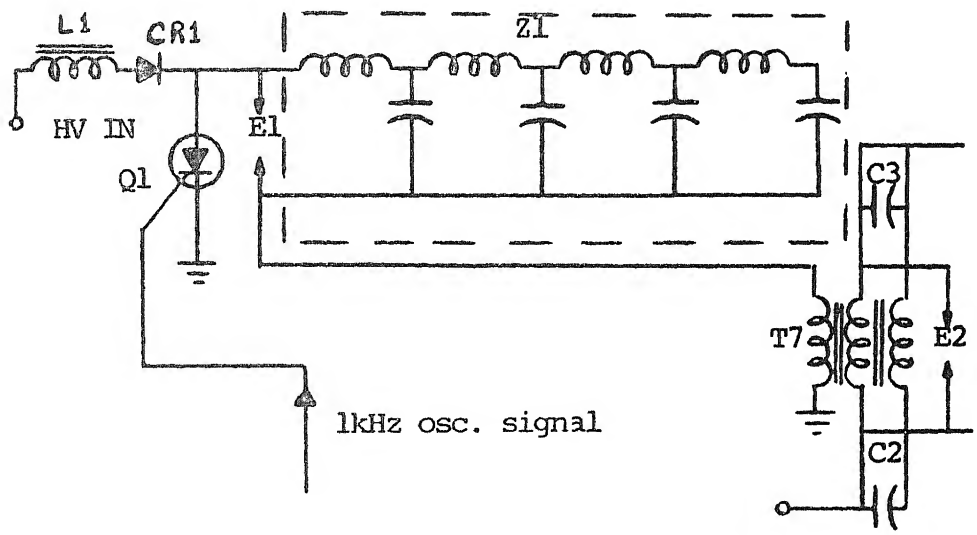
    b. Supplies the inverse current.

    c. L1 provides an inductive kick which nearly doubles the charge of the PFN.

    d. Supplies the bias voltage needed to operate Q2.

    e. Provides isolation of the PFN from the modulator power supply by limiting the rate of current flow during the charge cycle.

15. Select the components that are included in the charge path of the pulse forming network below.



PULSE FORMING NETWORK

a. Q1 and E1.

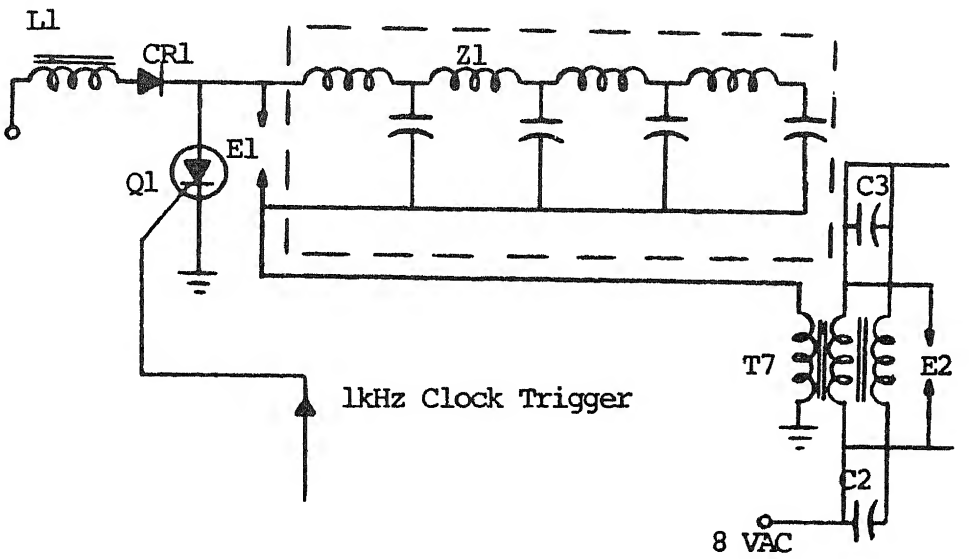
b. C3 and E2.

c. T-7 secondary, C2.

d. T-7 primary, Z1, CR1, L1.

e. T-7 primary, secondary and C2.

16. Which components are in the discharge path of the pulse forming network?



PULSE FORMING NETWORK

a. Secondary T-7, C2.

b. Primary T-7, Q1, Z1.

c. Primary T-7, C2, E1.

d. C3, E1, T-7.

17. Select the statement that describes the function of the holding diode (CR1).

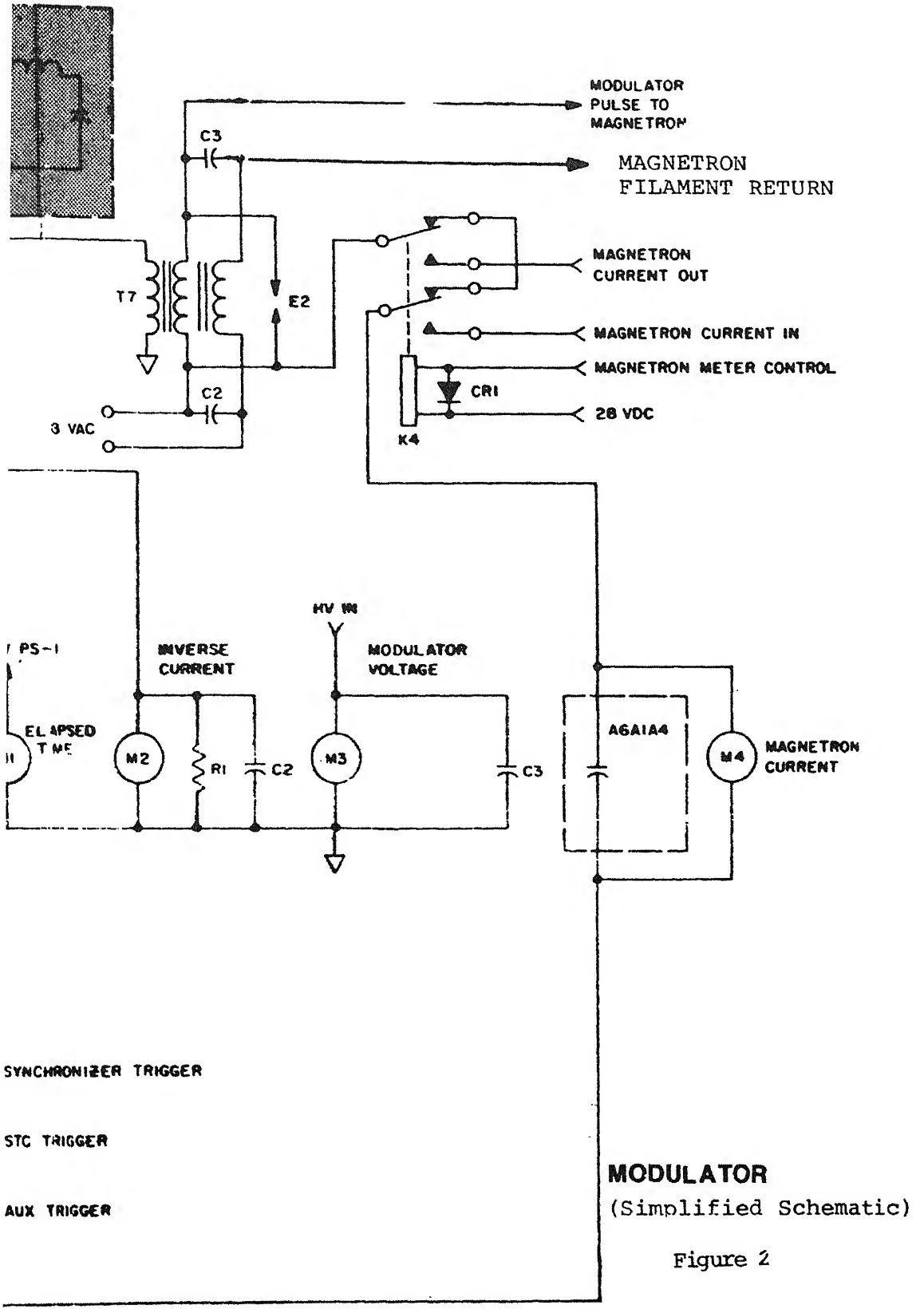
a. Keeps K3 deenergized all the time.

b. Allows the PFN to discharge.

c. Prevents the discharge of the PFN back through the Modulator Power Supply.

e. Applies a pulse to magnetron current meter M4.

You have completed this lesson topic. Report to your Learning Supervisor for the laboratory assignment.



MODULATOR
(Simplified Schematic)

Figure 2

LESSON TOPIC PROGRESS CHECK GUIDE

PULSE FORMING NETWORK AND SCR CONTROL CIRCUITS

TEST ITEMS ANSWERS	PRESCRIPTIVE STUDY GUIDE		
	SUMMARY PAGE(s)	NARRATIVE PAGE(s)	P. I. FARME(s)
1. c.			1
2. e.			3
3. b, c.			6
4. b.			9
5. d.			14
6. d.			16
7. a.			19
8. b.			22
9. a, b, d.			25
10. a, b.			28
11. d.			31
12. b.			34
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14. c, e.			41
15. d.			43
16. b.			46
17. c.			49

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LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

PULSE TRANSFORMER NETWORK

1. Which two statements describe the functions of a pulsed transformer with bifilar windings?

   a. Steps up the output of the PFN to a level sufficient to operate the magnetron.

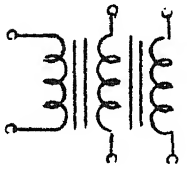
   b. Isolates the modulator pulse from the filament source voltage.

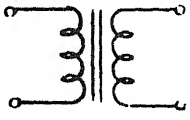
   c. Steps up the filament voltage to the magnetron.

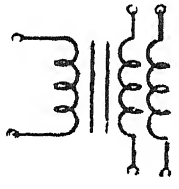
   d. Isolates the magnetron meter network from filament voltages.

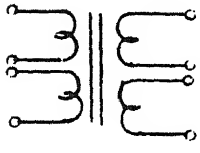
   e. Steps down the PFN voltage in order to increase current level for proper magnetron operation.

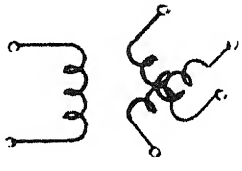
2. The two schematic symbols of a pulse transformer with a bifilar secondary windings are

a. 

b. 

c. 

d. 

e. 

3. The two symbols for a spark gap device are:

a. 

b. 

c. 

d. 

e. 

4. Spark gaps are used to protect circuit components in the modulator/transmitter from excessive current by

a. limiting the maximum voltage.

b. limiting the minimum voltage.

c. providing impedance matching.

d. preventing oscillations in the pulse transformer.

e. disabling the high voltage power supply.

5. The primary of the pulse transformer is connected to which component(s)?

   a. Z1

   b. A1, Q1.

   c. E1, Q1, and Z1.

   d. 8 vac.

6. The secondary (bilifar) windings of the pulse transformer are connected to which component(s)?

a. 1.	(1) E1.
b. 2, 3, 4.	(2) E2.
c. 1, 5.	(3) C2, C3.
d. 2, 5.	(4) J7, K4, 8 vac filament source.
e. 3, 5.	(5) A1, Z1.

You have completed this lesson topic. Report to your Learning Supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

PULSE TRANSFORMER NETWORK

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1. a, b.			1
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4. a.			10
5. c.			13
6. b.			16

LESSON TOPIC PROGRESS CHECK
(SELF-TEST)

MAGNETRON

1. A magnetron is:

   a. a triode.

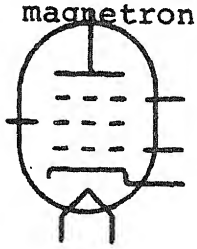
   b. a device containing inductors and capacitors which form tank circuits.

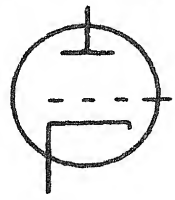
   c. a microwave power oscillator.

   d. a device that cannot be tuned to a specific frequency.

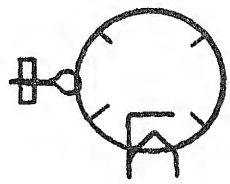
   e. an oscillator of only one type of construction.

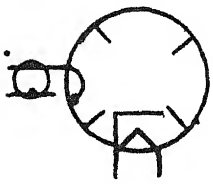
2. Select two schematic symbols for fixed tuned magnetrons.

   a. 

   b. 

   c. 

   d. 

   e. 

3. The function of a magnetron is:

   a. to produce a high power output in the microwave frequency.

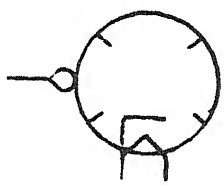
   b. to aid in charging the pulse transformer network.

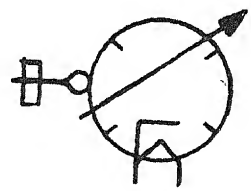
   c. to provide +280vdc for the pulse forming network.

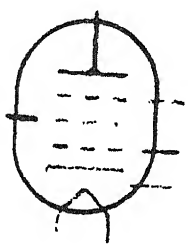
   d. to provide coupling between two i-f stages.

   e. to serve as a low Q oscillator.

4. The schematic symbol for a tunable magnetron is:

a. 

b. 

c. 

d. 

e. 

5. The pulse applied to the magnetron to initiate the microwave oscillations is

   a. blanking pulse.

   b. modulator pulse.

   c. low voltage pulse.

   d. synchronizer pulse.

   e. STC trigger.

6. Refer to the schematic of the modulator-power supply group. The modulator pulse applied to the cathode of the magnetron is directly coupled from:

   a. the pulse transformer primary.

   b. the pulse transformer secondary.

   c. the pulse forming network.

   d. the inverse current sensing network.

   e. inductor L1.

You have completed this lesson topic. Report to your Learning Supervisor for the laboratory assignment.

LESSON TOPIC PROGRESS CHECK GUIDE

MAGNETRON AND MAGNETRON CIRCUITS

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